Online Examinations (Even Sem/Part-I/Part-II Examinations 2020 - 2021

Course Name - Computer Organization and Architecture/ Computer Architecture and Organization
Course Code - BCA203

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Answer all the questions. Each question carry one mark.

9. 1. The addressing mode used in an instruction of the form ADD X, Y, is

Mark only one oval.

- [ ] absolute
- [ ] immediate
- [ ] Relative
- [ ] indirect

10. 2. The ability to temporarily halt the CPU and use this time to send information on buses is called

Mark only one oval.

- Direct memory access
- Vectoring the interrupt
- System Interrupt
- Cycle stealing

11. 3. Pseudo-instructions are

Mark only one oval.

- Assembler directives
- Instructions in any program that have corresponding machine code instruction
- Instruction in any program whose absence will not change the output for any input
- None of these

12. 4. addressing mode used in the instruction PUSH B is

Mark only one oval.

- Direct
- Register
- Register indirect
- Index

13. 5. The CPU of a Computer takes instruction from the memory and executes them. This process is called

Mark only one oval.

- Load cycle
- Time sequence
- Fetch-execute cycle
- None of these

14. 6. The unit of a computer system which executes program, communicates with and often controls the operation of other subsystems of the computer is the

Mark only one oval.

- CPU
- Control unit
- both CPU & Control unit
- Peripheral unit

15. 7. The control unit controls other units by generating _____

Mark only one oval.

- Control signals
- Timing signals
- Transfer signals
- Command Signals

16. 8. The addressing mode used in the instruction MOV A,B is

Mark only one oval.

- Direct
- Register
- Register indirect
- Index

17. 9. Which of the following addressing modes is used in instruction RAL

Mark only one oval.

- Immediate
- Implied
- Direct
- Register

18. 10. In the case of, Zero-address instruction method the operands are stored in _____

Mark only one oval.

- Registers
- Accumulators
- Push down stack
- Cache

19. 11. Operations of computer arithmetic and logic unit are directed by

Mark only one oval.

- ALU itself
- program
- control unit
- memory unit

20. 12. In a computer, ALU can perform

Mark only one oval.

- addition
- subtraction
- multiplication
- all of these

21. 13. Which representation is most efficient to perform arithmetic operations on the numbers?

Mark only one oval.

- Sign-magnitude
- 1's complement
- 2'S complement
- none of these

22. 14. When we subtract -3 from 2, the answer in 2's complement form is _____.

Mark only one oval.

- 0001
- 1101
- 0101
- 1001

23. 15. What is the binary equivalent of the decimal number 368?

Mark only one oval.

- 101110000
- 110110000
- 111010000
- 111100000

24. 16. 1's complement representation of decimal number of -17 by using 8 bit representation is

Mark only one oval.

- 1110 1110
- 1101 1101
- 1100 1100
- 0001 0001

25. 17. In a positive logic system, logic state 1 corresponds to

Mark only one oval.

- positive voltage
- higher voltage level
- zero voltage level
- lower voltage level

26. 18. The 2's complement of the number 1101110 is

Mark only one oval.

- 0010001
- 0110001
- 0010010
- None of these

27. 19. How can you represent a decimal point?

Mark only one oval.

- By weight decided by its position
- By a series of coefficients
- By location as well as base
- None of these

28. 20. Which sign bit is used for representing the positive sign in floating point representation?

Mark only one oval.

- 0
- 1
- either 1 or 0
- None of these

29. 21. Overflow occurs when

Mark only one oval.

- Data is out of range
- Data is within range
- both Data is out of range Data is within range
- None of these

30. 22. Which method/methods of representation of numbers occupies a larger amount of memory than others?

Mark only one oval.

- Sign-magnitude
- 1's complement
- 2's complement
- 1's & 2's complement

31. 23. The final addition sum of the numbers, 0111 & 0110 is _____

Mark only one oval.

- 1101
- 1111
- 1001
- 1010

32. 24. The advantage of I/O mapped devices to memory mapped is

Mark only one oval.

- The former offers faster transfer of data
- The devices connected using I/O mapping have a bigger buffer space
- The devices have to deal with fewer address lines
- No advantage as such

33. 25. The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is

Mark only one oval.

- Exceptions
- Signal handling
- Interrupts
- DMA

34. 26. The principle of locality justifies the use of

Mark only one oval.

- Interrupt
- DMA
- Polling
- Cache memory

35. 27. Physical memory broken down into groups of equal size is called

Mark only one oval.

- Page
- block/frame
- tag
- index

36. 28. Micro Instruction are kept in

Mark only one oval.

- Main memory
- Control memory
- Cache memory
- Auxiliary memory

37. 29. Which registers can interact with the secondary storage?

Mark only one oval.

- MAR
- PC
- IR
- RO

38. 30. The effectiveness of the cache memory is based on the property of _____

Mark only one oval.

- Locality of reference
- Memory localization
- Memory size
- None of the mentioned

39. 31. During a write operation if the required block is not present in the cache then _____ occurs.

Mark only one oval.

- Write latency
- Write hit
- Write delay
- Write miss

40. 32. The memory blocks are mapped on to the cache with the help of _____

Mark only one oval.

- Hash functions
- Vectors
- Mapping functions
- None of the mentioned

41. 33. The number successful accesses to memory stated as a fraction is called as _____

Mark only one oval.

- Hit rate
- Miss rate
- Success rate
- Access rate

42. 34. The smallest entity of memory is called _____

Mark only one oval.

- Cell
- Block
- Instance
- Unit

43. 35. Execution of several activities at the same time is called-

Mark only one oval.

- processing
- parallel processing
- serial processing
- multitasking

44. 36. A pipeline is like-

Mark only one oval.

- an automobile assembly line
- house pipeline
- Bothan automobile assembly line & house pipeline
- a gas line

45. 37. Which of the following bus is used to transfer data from the main memory to peripheral devices?

Mark only one oval.

- DMA bus
- Output bus
- Data bus
- All of these

46. 38. Instruction pipelining has minimum_____ stages

Mark only one oval.

- 4
- 2
- 3
- 6

47. 39. A collection of lines that connects several devices is called-

Mark only one oval.

- peripheral connection wires
- bus
- Internal wires
- both bus & peripheral connection wires

48. 40. The transfer of large chunks of data with the involvement of the processor is done by-

Mark only one oval.

- DMA controller
- Arbitrator
- User system programs
- None of the mentioned

49. 41. An instruction code must specify the address of the-

Mark only one oval.

- Operand
- Opcode
- Both of above
- None of above

50. 42. User programs interact with I/O devices through?

Mark only one oval.

- Operating System
- Hardware
- Buses
- Processor

51. 43.If the CPU and I/O interface share a common bus than transfer of data between two units is known as?

Mark only one oval.

- Asynchronous
- Clock dependent
- Synchronous
- Decoder independent

52. 44. A set of physical addresses is also known as-

Mark only one oval.

- Disk Space
- Address Space
- Memory Space
- Locations

53. 45. Which table handles store address of interrupt handling subroutine?

Mark only one oval.

- Vector table
- Symbol link table
- Interrupt vector table
- None of above

54. 46. Which technique has one or more control signal for acknowledgement that is used for intimation?

Mark only one oval.

- FTP
- Ping
- Strobe
- Handshaking

55. 47. How many RAM chips of size (256 X 1bit) are required to build (1024 X 1bit) Memory?

Mark only one oval.

- 24
- 4
- 32
- 8

56. 48. Why do we need to have secondary storage?

Mark only one oval.

- Store large volume of data that exceed the capacity of main memory
- Perform arithmetic and logical operations
- To give power to the system too
- To help processor in processing

57. 49. The bit used to signify that the cache location is updated is _____

Mark only one oval.

- Dirty bit
- Update bit
- Reference bit
- Flag bit

58. 50. The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____

Mark only one oval.

- Set associative
- Associative
- Direct
- Indirect

59. 51. In associative mapping, in a 16 bit system the tag field has _____ bits.

Mark only one oval.

- 12
- 8
- 9
- 10

60. 52. The reason for the implementation of the cache memory is _____

Mark only one oval.

- To increase the internal memory of the system
- The difference in speeds of operation of the processor and memory
- To reduce the memory access and cycle time
- All of the mentioned

61. 53. The collection of the entities where data is stored is called _____

Mark only one oval.

- Block
- Set
- Word
- Byte

62. 54. A term for simultaneous access to a resource, physical or logical.

Mark only one oval.

- Multiprogramming
- Multitasking
- Threads
- Concurrency

63. 55. _____ leads to concurrency.

Mark only one oval.

- Serialization
- Parallelism
- Serial processing
- Distribution

64. 56. A parallelism based on increasing processor word size.

Mark only one oval.

- instructional
- bit level
- bit based
- increasing

65. 57. The rate at which the problem size needs to be increased to maintain efficiency.

Mark only one oval.

- Isoefficiency
- Efficiency
- Scalability
- Effectiveness

66. 58. CPU does not perform the operation, called

Mark only one oval.

- data transfer
- logic operation
- arithmetic operation
- all of the above

67. 59. From where interrupts are generated?

Mark only one oval.

- Central processing unit
- Memory chips
- Registers
- I/O devices

68. 60. PC or Program Counter is also called

Mark only one oval.

- instruction pointer
- memory pointer
- file pointer
- data counter

69. 61. The internal components of the processor are connected by-

Mark only one oval.

- Processor intra-connectivity circuitry
- Processor bus
- Memory bus
- Rambus

70. 62. Which method of representation has two representations for ‘0’?

Mark only one oval.

- Sign-magnitude
- 1’s complement
- 2’s complement
- None of the mentioned

71. 63. An exception condition in a computer system caused by an event external to the CPU is known as?

Mark only one oval.

- Halt
- Process
- Interrupt
- None of above

72. 64. Whenever a CPU detects an interrupt, what does it do with current state?

Mark only one oval.

- Save it
- Discard it
- Depends system to system
- First finish it

73. 65. I/O processor has direct access to-

Mark only one oval.

- Main Memory
- Secondary Memory
- Flash Memory
- ROM

74. 66. Which among the following is an important data transfer technique?

Mark only one oval.

- CAD
- CAM
- DMA
- MMA

75. 67. The decoded instruction is stored in _____

Mark only one oval.

- IR
- PC
- Registers
- MDR

76. 68. The internal components of the processor are connected by _____

Mark only one oval.

- Processor intra-connectivity circuitry
- Processor bus
- Memory bus
- Rambus

77. 69. The eliminating stage of WAR and WAW hazards, is often called

Mark only one oval.

- Execution
- Anti-dependence
- Data hazards
- Dispatch

78. 70. The actual data flow values among instructions, which produce results and those that consume those results, is known as

Mark only one oval.

- Control flow
- Control hazard
- Data hazard
- Data flow