Online Examinations (Even Sem/Part-I/Part-II Examinations 2020 - 2021

Course Name - Computer Organization and Architecture Course Code - BCAC202

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_ .. . _ _

- PGDHM
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Answer all the questions. Each question carry one mark.

9. 1. Which representation is most efficient to perform arithmetic operations on the numbers?

- Sign-magnitude
- 2'S complemen
- none of these

10. 2. Which registers can interact with the secondary storage?

Mark only one oval.



11. 3. Which table handles store address of interrupt handling subroutine?

Mark only one oval.

- Vector table
- Symbol link table
- Interrupt vector table
- None of above
- 12. 4. PC or Program Counter is also called

- instruction pointer
- ____ memory pointer
- file pointer
- 🔵 data counter

13. 5. Processor without structural hazard is

Mark only one oval.

Faster

Slower

- Have longer clock cycle
- ____ have larger clock rate
- 14. 6. In the case of, Zero-address instruction method the operands are stored in _____

Mark only one oval.

\bigcirc	Registers
\bigcirc	Accumulators
\bigcirc	Push down stack
\bigcirc	Cache

15. 7. The principle of locality justifies the use of

Mark only one oval.

DMA

Polling

Cache memory

16. 8. User programs interact with I/O devices through?

Mark only one oval.

Operating System
Hardware
Buses
Processor

17. 9. The rate at which the problem size needs to be increased to maintain efficiency

Mark only one oval.



18. 10. Ideal CPI (Cycle per instruction) on a pipelined processor is almost always

Mark only one oval.



______ 4

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19. 11. The control unit controls other units by generating _____

Mark only one oval.

- Control signals
- Timing signals
- Transfer signals
- Command Signals
- 20. 12. The final addition sum of the numbers, 0111 & 0110 is _____

Mark only one oval.

- 1101

- 21. 13. A collection of lines that connects several devices is called-

Mark only one oval.

____ peripheral connection wires

bus

- 🔵 Internal wires
- both bus & peripheral connection wires

22. 14. A term for simultaneous access to a resource, physical or logical.

Mark only one oval.

\bigcirc	Multiprogramming
\bigcirc	Multitasking
\bigcirc	Threads
\bigcirc	Concurrency

23. 15. The actual data flow values among instructions, which produce results and those that consume those results, is known as

Mark only one oval.

\bigcirc	Control	flow
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- Control hazard
- 🔵 Data hazard
- Data flow
- 24. 16. addressing mode used in the instruction PUSH B is

Mark only one oval.

Direct

- Register
- Register indirect
- 🔵 Index

25. 17. Which sign bit is used for representing the positive sign in floating point representation?

Mark only one oval.

\bigcirc	0
\bigcirc	1
\bigcirc	either 1 or 0
\bigcirc	None of these

26. 18. A pipeline is like-

Mark only one oval.

an automobile assembly line

house pipeline

Bothan automobile assembly line & house pipeline

- 🔵 a gas line
- 27. 19. The reason for the implementation of the cache memory is _____

- To increase the internal memory of the system
- The difference in speeds of operation of the processor and memory
- To reduce the memory access and cycle time
- All of the mentioned

28. 20. The decoded instruction is stored in _____

Mark only one oval.

\bigcirc	IR
\bigcirc	PC
\bigcirc	Registers
\bigcirc	MDR

29. 21. The addressing mode used in an instruction of the form ADD X, Y, is

Mark only one oval.

- absolute
- Relative
- indirect
- 30. 22. In a positive logic system, logic state 1 corresponds to

- ____ positive voltage
- higher voltage level
- ____ zero voltage level
- 🔵 lower voltage level

31. 23. The number successful accesses to memory stated as a fraction is called as

Mark only one oval.

Hit rate
 Miss rate
 Success rate
 Access rate

32. 24. The bit used to signify that the cache location is updated is _____

Mark only one oval.

\bigcirc	Dirty	bit	
------------	-------	-----	--

Update bit

Reference bit

- 🔵 Flag bit
- 33. 25. Whenever a CPU detects an interrupt, what does it do with current state?

Mark only one oval.

🔵 Save it

Discard it

Depends system to system

🕖 First finish it

34. 26. When we subtract -3 from 2, the answer in 2's complement form is _____.

Mark only one oval.

35. 27. The effectiveness of the cache memory is based on the property of _____

Mark only one oval.

Locality of reference
 Memory localization
 Memory size
 None of the mentioned

36. 28. Which technique has one or more control signal for acknowledgement that is used for intimation?

Mark only one oval.

FTP

Ping

- Strobe
- Handshaking

37. 29. The internal components of the processor are connected by-

Mark only one oval.

- Processor intra-connectivity circuitry
- Processor bus
- Memory bus
- 🔵 Rambus
- 38. 30. Hazards in pipelined stages are of

Mark only one oval.

- 🔵 Two types
- Three types
- Four types
- Five types
- 39. 31. Operations of computer arithmetic and logic unit are directed by

Mark only one oval.

ALU itself

____ program

- control unit
- memory unit

40. 32. Physical memory broken down into groups of equal size is called

Mark only one oval.

Page
block/frame
tag
index

41. 33. If the CPU and I/O interface share a common bus than transfer of data between two units is known as?

Mark only one oval.

\bigcirc	Asynchronous
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- Clock dependent
- Synchronous
- Decoder independent
- 42. 34. CPU does not perform the operation, called



- logic operation
- arithmetic operation
- all of the above

43. 35. If event occurs at same place every time program is executed with same data and memory allocation, then event is known as

Mark only one oval.

- Asynchronous
- Synchronous
- Delayed
- Stalled
- 44. 36. The addressing mode used in the instruction MOV A,B is

\bigcirc	Direct
\bigcirc	Register
\bigcirc	Register indirect
\bigcirc	Index

Mark only one oval.

45. 37. The advantage of I/O mapped devices to memory mapped is

- The former offers faster transfer of data
- The devices connected using I/O mapping have a bigger buffer space
- The devices have to deal with fewer address lines
- No advantage as such

46. 38. The transfer of large chunks of data with the involvement of the processor is done by-

Mark only one oval.

- DMA controller
- Arbitrator
- User system programs
- None of the mentioned
- 47. 39. _____ leads to concurrency.

Mark only one oval.

- Serialization
- Parallelism
- Serial processing
- Distribution
- 48. 40. Between the instruction ADD D and the instruction SUB D, there is



- Anti-dependence
- Correlation
- Scheduling

49. 41. The CPU of a Computer takes instruction from the memory and executes them. This process is called

Mark only one oval.

Load cycle

- Time sequence
- Fetch-execute cycle
- None of these
- 50. 42. Overflow occurs when

Mark only one oval.

Data is out of range

Data is within range

both Data is out of range Data is within range

None of these

51. 43. Which of the following bus is used to transfer data from the main memory to peripheral devices?

- DMA bus
- Output bus
- 🔵 Data bus
- All of these

52. 44. The collection of the entities where data is stored is called _____

Mark only one oval.

\bigcirc	Block
\bigcirc	Set
\bigcirc	Word
\bigcirc	Byte

53. 45. The internal components of the processor are connected by _____

Mark only one oval.

Processor intra-connectivity circuitry

Processor bus

Memory bus

- 📃 Rambus
- 54. 46. The ability to temporarily halt the CPU and use this time to send information on buses is called

Mark only one oval.



Vectoring the interrupt

System Interrupt

Cycle stealing

55. 47. The 2's complement of the number 1101110 is

Mark only one oval.

0010001
 0110001
 0010010
 None of these

56. 48. The smallest entity of memory is called _____

Mark only one oval.

- Cell
 Block
 Instance
- Unit
- 57. 49. The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____

- Set associative
- Associative
- Direct
- Indirect

58. 50. What is the binary equivalent of the decimal number 368?

Mark only one oval.

0101110000

_____ 110110000

111010000

111100000

59. 51. I/O processor has direct access to-

Mark only one oval.

- Main Memory
- Secondary Memory

Flash Memory

ROM

60. 52. During a write operation if the required block is not present in the cache then _____ occurs.

Mark only one oval.

Write latency

Write hit

- Write delay
- Write miss

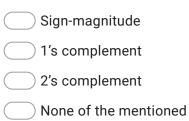
61. 53. How many RAM chips of size (256 X 1bit) are required to build (1024 X 1bit) Memory?

Mark only one oval.

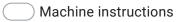


62. 54. Which method of representation has two representations for '0'?

Mark only one oval.



63. 55. In micro-programmed approach, the signals are generated by _____



- System programs
- Utility tools
- None of the mentioned

64. 56. In a computer, ALU can perform

Mark only one oval.

addition

- subtraction
- ____ multiplication
- all of these
- 65. 57. Micro Instruction are kept in

Mark only one oval.

- Main memory
- Control memory
- Cache memory
- Auxiliary memory
- 66. 58.A set of physical addresses is also known as-

Mark only one oval.

🔵 Disk Space

Address Space

Memory Space

Locations

67. 59. From where interrupts are generated?

Mark only one oval.

- Central processing unit
- Memory chips
- Registers
- I/O devices
- 68. 60. Sum of contents in a base register and sign-extended offset is used as a memory address, sum is known as

Mark only one oval.

- ALU instructions
- Throughput
- Effective address
- Load and store instructions

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