Online Examinations (Even Sem/Part-I/Part-II Examinations 2020 - 2021

Course Name - - Microprocessors Course Code - DCSE404

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9.

DIP.ME
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M.A.(JMC)
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M.SC.(ANCS)
M.SC.(MM)
B.A.(Eng)
Answer all the questions. Each question carry one mark.
. 1. Why 8085 Processor is called an 8-bit processor?
Mark only one oval.
Because 8085 processor has 8-Bit ALU.
Because 8085 processor has 8-Bit control bus.
Because 8085 processor has 8-Bit data bus.
None of these

10.	2. Microprocessor speed depends on which parameter?
	Mark only one oval.
	Clock
	Address Bus Width
	Data Bus Width
	None of these
11.	3. Which of the following is a user programmable register?
	Mark only one oval.
	Memory Address Register
	Data Register
	Accumulator
	Program Counter
12.	4. Why 8085 processor is called an 8 bit processor?
	Mark only one oval.
	Because 8085 processor has 8 bit ALU.
	None of these
	Because 8085 processor has 8 bit data bus.
	Both (a) and (b)

13.	5. Name of the program responsible to transfer hex input to binary is
	Mark only one oval.
	System Program Application Program Monitor Program Compiler
14.	6. HLT is a operation
	Mark only one oval.
	Data transfer Arithmetic Machine Control Branching
15.	7. JNZ is one kind of operation Mark only one oval.
	Data transfer Arithmetic Branching Machine Control

16.	8. PSW in 8085 microprocessor is a
	Mark only one oval.
	4-bit register
	8-bit register
	16-bit register
	12-bit register
17.	9. How many T-States are there in STA 8050H instruction?
	Mark only one oval.
	10
	9
	<u> </u>
18.	10. Who is the last machine cycle in LDA 2030H?
	Mark only one oval.
	Op-code Fetch
	Memory Write
	Memory Read
	I/O Read

19.	11. Full form of SIM is
	Mark only one oval.
	Select Interrupt Mask Sorting Interrupt Mask Set Interrupt Mask None of these
20.	12. Addressing mode of STA 8055H instruction is
	Mark only one oval.
	Immediate Implied Memory Direct Stack
21.	13. The interrupt line having highest priority is
	Mark only one oval.
	RST 7.5 RST 6.5 TRAP SLEEP

22.	14. How many instructions are present in 8085 instruction set?
	Mark only one oval.
	75
	77
	78
23.	15. DAD is a
	Mark only one oval.
	Instruction
	Register
	Operation
	None of these
24.	16. An interrupt that can be turned off by the programmer is known as
	Mark only one oval.
	Non-Maskable Interrupt
	Software Interrupt
	Maskable Interrupt
	Priority Interrupt

25.	17. For MOV A, M instruction, one of the operand will be stored in
	Mark only one oval.
	HL Address of operand will be stored in HL Accumulator None of these
26.	18. Which statement is true for MOV D, B instruction?
	Mark only one oval.
	2 -Byte Instruction 3 -Byte Instruction 1 -Byte Instruction 4 -Byte Instruction
	4 Byte instruction
27.	19. Addressing mode of PUSH B instruction is
	Mark only one oval.
	Immediate
	Implied
	Stack
	Register Direct

	28.	20. Jumping from one location to another unconditionally can be done by
		Mark only one oval.
		JNZ JZ JMP
	29.	21. Which instruction is not present in 8085 instruction set?
		Mark only one oval.
		ADD SUB MULT ORA
;	30.	22. The program counter in a 8085 micro-processor is a 16-bit register, because Mark only one oval. It counts 16-bits at a time
		It facilitates the user storing 16-bit data temporarily There are 16 address lines It has to fetch two 8-bit data at a time

31.	23. In Intel 8085A microprocessor ALE signal is made high to		
	Mark only one oval.		
	To latch data D0-D7 from data bus		
	To disable data bus		
	Enable the data bus to be used as low order address bus		
	To achieve all the functions listed above		
32.	24. CALL instruction is a instruction.		
	Mark only one oval.		
	2 Byte		
	3 Byte		
	1 Byte		
	4 Byte		
33.	25. The advantage of memory mapped I/O over I/O mapped I/O is		
	Mark only one oval.		
	Faster		
	Require a bigger address decoder		
	Many instructions supporting memory mapped I/O		
	All the above		

34.	26. If 300 peripheral device need to be interfaced with 8085, which should be preferred?
	Mark only one oval.
	Memory-mapped I/OPeripheral-mapped I/O
	Any one
	Memory-mapped I/O
	None of these
35.	27. Number of Hex digits needed to represent the 16-bit address of a memory location are
	Mark only one oval.
	3
	5
	4
	<u> </u>
36.	28. 8005H location can be used as a peripheral address in which method?
	Mark only one oval.
	Peripheral -mapped I/O
	Any one
	Memory-mapped I/O
	None of these

37.	29. Third state of a tri-state device is 29. The average number of comparisons performed by merge sort algorithm in merging two sorted lists of 2 elements is
	Mark only one oval.
	High
	Low
	High-Impedance
	Both a and b
38.	30. Memory-mapped and peripheral mapped I/O are related to
	Mark only one oval.
	Memory Interfacing
	Both a and b
	Peripheral Interfacing
	None of these
39.	31. Total addressable memory location supported by Intel 8086 is
	Mark only one oval.
	28
	210
	216
	220

40.	32. Full form of OF in Intel 8086 microprocessor is
	Mark only one oval.
	Overdue Flag
	One Flag
	Overflow Flag
	Over Flag
41.	33. in Intel 8086 microprocessor, the work of EU is
	Mark only one oval.
	Decoding
	Processing
	Encoding
	Calculation
42.	34. The RD, WR, M/IO are the heart of control for mode
	Mark only one oval.
	Maximum
	Halt
	Minimum
	Fetch

43.	35. Intel 8086 is a bit microprocessor
	Mark only one oval.
	8
	10
	<u> </u>
	20
44.	36. Register AX is formed by grouping
	Mark only one oval.
	AH and AL
	BH and BL
	CH and CL
	DH and DL
45.	37. Microprocessor determines whether specified condition exists or not by testing
	Mark only one oval.
	Carry Flag
	Common Flag
	Conditional Flag
	Sign Flag

46.	38. If MN/MX is low, 8086 operates on mode
	Mark only one oval.
	Maximum
	Both a and b
	Minimum
	Medium
47.	39. The instruction, MOV AX, 1234H is an example of
	Mark only one oval.
	Register
	Direct
	Immediate
	Register Relative
48.	40. Which is not a machine cycle?
	Mark only one oval.
	Op-code Fetch
	Memory Read
	None of these
	I/O Read

49.	41. Which one requires 4 t-States to complete?
	Mark only one oval.
	Memory Read
	I/O Write
	Op-code Fetch
	Memory Write
50.	42. Which stack is used in 8085?
	Mark only one oval.
	LIFO
	FILO
	FIFO
	None of these
	Notice of these
51.	43. Which one has the highest priority
	Mark only one oval.
	TRAP
	RST 7.5
	HOLD
	☐ INTR

52.	44. Addressing mode of MOV A, B is
	Mark only one oval.
	Memory Direct
	Memory Indirect
	Register Direct
	Base Register
53.	45. Stack Pointer is a register
	Mark only one oval.
	4 bit
	16 bit
	8 bit
	None of these
54.	46. After XRA A, content of A will be always
	Mark only one oval.
	O
	1
	2
	<u>3</u>

55.	47. Addressing mode of HLT instruction is
	Mark only one oval.
	Immediate
	Implied
	Stack
	Register Direct
56.	48. Which flag is associated with JNC 8050H instruction?
	Mark only one oval.
	Zero
	Sign
	Carry
	Parity
- 7	40 M/sich flowing and sinted with INIZ 005011 inchwesting?
57.	49. Which flag is associated with JNZ 8050H instruction?
	Mark only one oval.
	Sign
	Parity
	Zero
	Carry

58.	50. Which of the following instruction is not possible in 8085?
	Mark only one oval.
	OPOP PSW
	POP B
	POP 30H
	POP D
59.	51. Which general/special register or general/special register pair is incremented decremented by 2 during PUSH and POP instructions?
	Mark only one oval.
	HL
	□ DE
	Stack Pointer
	Program Counter
60.	52. To interface a memory with 2048 locations, how many address lines will be used?
	Mark only one oval.
	10
	11
	12
	<u> </u>

61.	53. Maximum numbers of addresses supported by peripheral-mapped-I/O is
	Mark only one oval.
	128 256 512 1024
62.	54. Which among is a peripheral-mapped-I/O instruction?
	Mark only one oval.
	LDA
	STA
	◯ IN
	None of these
63.	55. More than one address of an device is possible with
	Mark only one oval.
	Absolute Decoding
	Both a and b
	Partial Decoding
	None of these

64.	56. To interface a memory with 1024 locations, how many address lines will be used?		
	Mark only one oval.		
	11		
	12		
	10		
	16		
65.	57. 2732 is a IC of		
	Mark only one oval.		
	Decoder		
	R/W memory		
	EPROM		
	RAM		
66.	58. Data bus width of Intel 8086 is		
	Mark only one oval.		
	10 bit		
	8 bit		
	16 bit		
	20 bit		

67.	59. The is used to connect more microprocessor
	Mark only one oval.
	Peripheral
	I/O devices
	Cascade
	Control unit
68.	60. The index register is used to hold
	Mark only one oval.
	Memory Register
	Offset Register
	Offset Memory
	Segmented Memory

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