Online Examinations (Even Sem/Part-I/Part-II Examinations 2020 - 2021

Course Name - - Microprocessors Course Code - DECE404

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Answer all the questions. Each question carry one mark.

9. 1. The memory capacity of 8085 microprocessor is

- ____ 64 KB
- 1 MB
- _____ 16 MB
- 640 B

10. 2.8085 microprocessor has how many pins

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11. 3. Which of the following microprocessors is a 4 bit microprocessor?

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- 4004
 8080
 8085
 8086
- 12. 4. In 8085 microprocessor, name the 16 bit register is called



- Both Stack Pointer and PSW
- None of these

13. 5. In a computer where microprocessor is used as CPU is known as

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Microprocessor

- Micro-computer
- Microcontroller
- All of these
- 14. 6. An 8-bit microprocessor has an

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- 🔵 8 bit data bus
- 8-bit address bus
- 8-bit control bus
- 🔵 8-bit interrupt lines
- 15. 7. Which semiconductor technology is used for fabrication of 8085 microprocessor?

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ECL

- NMOS and HMOS
- NMOS and CMOS

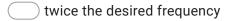
 8. If the microprocessor is capable of addressing 1MB of memory, its address bus width is

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16 bits
20 bits
8 bits

- none of these
- 17. 9. The frequency of the driving network connected between pins 1 and 2 of 8085 microprocessor is

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- equal to the desired frequency
- _____ four times the desired frequency
- none of these
- 18. 10. Why 8085 processor is called an 8 bit processor?

- because 8085 processor has 8 bit ALU
- because 8085 processor has 8 bit data bus
- because 8085 processor has 16 bit data bus
- because 8085 processor has 16 bit address bus

19. 11. A microprocessor is a

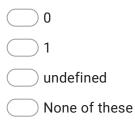
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SSI device

- MSI device
- LSI device
- VLSI device
- 20. 12. The address bus of microprocessor is

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- _____ unidirectional
- bi-directional
- unidirectional as well as bi-directional
- none of these
- 21. 13. After add 89H & 79H , the status of Parity flag will be



22. 14. Which one of the following is called non-vectored interrupt?

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23. 15. ADD C will be executed in

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- ____ 1 Machine cycle
- 2 Machine cycle
- 3 Machine cycle
- 4 Machine cycle
- 24. 16. What is SIM?

- Select Interrupt Mask
- Shoting Interrupt Mask
- 🔵 Set Interrupt Mask
- None of these

25. 17. The number of T-States required for PCHL instruction execution is

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26. 18. XCHG is an

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- 🔵 data transfer instruction
- logical instruction
- arithmatic instruction
- none of these
- 27. 19. The instruction "JUMP" belongs to

- sequential control flow instructions
- control transfer instructions
- branch instructions
- control transfer & branch instructions

28. 20. Which instruction is required to rotate the content of accumulator one bit right along with carry?

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- RLC RAL
 - RAR
- 29. 21. What are level Triggering interrupts?

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- 🔵 INTR & TRAP
- 🔵 RST6.5 & RST5.5
- 🔵 RST7.5 & RST6.5
- RST2.5 & RST6.2
- 30. 22. What are software interrupts?_____



- RST 5.5 7.5
- INTR, TRAP
- RST 4.4 6.4

31. 23. MOV A, C is an instruction of

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One byte

- two byte
- three byte
- _____ four byte
- 32. 24. CMA is an instruction of

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direct addressing mode

indirect addressing mode

register addressing mode

- Implicit addressing mode
- 33. 25. MVI A, 58H is an instruction of

- direct addressing mode
- indirect addressing mode
- register addressing mode
- Immediate addressing mode

34. 26. By issuing which one of the following signal, CPU releases the system bus to DMA controller?

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HOLD HLDA ALE READY

35. 27. The technique of assigning a memory address to each I/O device in the computer system is called:

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memory-mapped I/O
ported I/O
dedicated I/O
wired I/O

36. 28. In 8086 microprocessor, the size of each segment is

- 32 KB
- 64 KB
- _____ 16 KB
- 🔵 8 KB

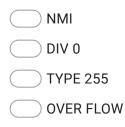
37. 29. In which year, 8086 microprocessor was introduced?

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38. 30. In 8086 microprocessor the following has the highest priority among all type interrupts?

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39. 31. 8088 microprocessor has

- 🔵 16 bit data bus
- _____ 4 byte pre-fetch queue
- 6 byte pre-fetch queue
- 📃 16 bit address bus

40. 32. What is addressing mode of instruction MOV AX, [BX]?

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register addressing mode

- immediate addressing mode
- _____ register indirect addressing mode
- indirect addressing mode
- 41. 33. Which of the following is based with 16 bit displacement addressing?

Mark only one oval.

- _____ MOV AX, [BX+06]
- MOV AX, [BP+2000]
- ____ MOV AX, [BP+06]
- MOV AX, [BP]
- 42. 34. Instruction queue of 8086 consist of

- 🔵 6 data
- 🛛 8 data
- ____ 4 data
- 🔵 10 data

43. 35. Segment memory capacity of 8086 is

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44. 36. Which of the following instruction is a logical instruction?

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45. 37. DS Stand for

- Data segment
- Direct segment
- Declare segment
- Divide segment

46. 38. How many register banks are present in 8051 microcontroller?

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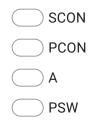


47. 39. Which of the following comes under the indexed addressing mode?

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48. 40. Which of the following registers are not bit addressable?



49. 41. When 8051 wakes up then 0x00 is loaded to which register?

Mark only one oval.



50. 42. Which of the following register can be used to hold address of byte in the memory of 8051?

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- PCON
- SBUF
- PSW
- 51. 43. The 8051 microcontroller is of ___pin package as a _____ processor.

- 30, 1byte
- 20, 1 byte
- _____ 40, 8 bit
- _____ 40, 8 byte

52. 44. JZ, JNZ, DJNZ, JC, JNC instructions monitor the bits of which register in 8051?

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53. 45. Which of the following instruction is incorrect?

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54. 46. Consider the following registers: a. Accumulator and flag register b. B and C register c. D and E register d. H and L register Which of these 8-bit registers of 8085 microprocessor can be paired together to make a 16-bit register?

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a,c,d
 b,c,d
 a,b,d
 a,b,c

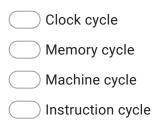
55. 47. Which stack is used in 8085?

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56. 48. The cycle required to fetch and execute an instruction in a 8085 microprocessor is which one of the following?

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57. 49. A sequence of two registers that multiplies the content of DE register pair by two and stores the result in HL register pair (in 8085 assembly language) is

- XCHG & DAD B
- XTHL & DAD H
- PCHL & DAD D
- 🔵 XCHG & DAD H

58. 50. MOV A,C is executed by

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one machine cycle

- 🔵 two machine cycle
- _____ three machine cycle
- four machine cycle
- 59. 51. IN OOH is an instruction of

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- direct addressing mode
- indirect addressing mode
- _____ register addressing mode
- Immediate addressing mode
- 60. 52. The 16 bit flag of 8086 microprocessor is responsible to indicate

- _____ the condition of result of ALU operation
- the condition of memory
- _____ the result of addition
- the result of subtraction

61. 53. OUT 00H is an instruction of

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- direct addressing mode
- indirect addressing mode
- register addressing mode
- Immediate addressing mode
- 62. 54. LHLD 2500H is an instruction of

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- direct addressing mode
- indirect addressing mode
- _____ register addressing mode
- Immediate addressing mode
- 63. 55. ADI, 01 H is an instruction of

- direct addressing mode
- indirect addressing mode
- register addressing mode
- Immediate addressing mode

64. 56. CMP B is an instruction of

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direct addressing mode

indirect addressing mode

register addressing mode

- Immediate addressing mode
- 65. 57. How many T-states are required for execution of LHLD 3600 H instruction?

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- 10
 13
 16
 7
- 66. 58. How many T-states are required for execution of MVI A, 05H instruction?

Mark only one oval.

10
4
7

) 13

67. 59. How many T-states are required for execution of JNZ 2602H instruction?

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68. 60. LXI H, 2500 H is executed by

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- _____ five machine cycle
- two machine cycle
- _____ three machine cycle
- _____ four machine cycle

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