# Online Examinations (Even Sem/Part-I/Part-II Examinations 2020 - 2021

Course Name - - Computer Organization and Architecture Course Code - PCC-CS401

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- PGDHM
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Answer all the questions. Each question carry one mark.

9. 1. Which of the following is a universal logic gate?

- OR

10. 2. Boolean algebra is also known as

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Counting algebra

Switching algebra

Transistor algebra

🔵 Gate algebra

11. 3. Which of the following is used to store intermediate result?

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Accumulator
MAR
MDR

Program Counter

12. 4. Which of the following is not a bus?\_\_\_\_.

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control bus

🔵 data bus

program bus

🔵 address bus

13. 5. Which of the following is used to store the address of next instruction?

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$\bigcirc$	Accumulator
$\bigcirc$	MAR
$\bigcirc$	Program Counter
$\bigcirc$	MDR

14. 6.A collection of lines that connects several devices is called

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peripheral connection wires
bus
Accumulator
Internal wires

15. 7.The instructions like MOV or ADD are called as

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OP-Code

Commands

Operators

None of above

16. 8.In which addressing mode the address of the operand is specified?

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Absolute

- Immediate
- Indirect
- Direct

# 17. 9. MRI indicates

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- Memory Reference Information
- Memory Reference Instruction
- Memory Registers Instruction
- Memory Register information
- 18. 10.Content addressable memory is also known as

- Main memory
- Virtual memory
- Associative memory
- Auxiliary memory

19. 11. Memory management technique where allocated size is fixed -

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paging

- segmentation
- fragmentation
- indexing
- 20. 12. Which of the following is/are type of multi processor on basis of memory?

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- Shared memory
- Distributed memory
- Both of these
- None of these
- 21. 13.Associative memory is ...... than RAM.

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faster same

slower

odes not depend

22. 14. Which of the following is/are the algorithm for page replacement?

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23. 15. If the required page is not present in the main memory, it is said to be

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- Page hit
  Page fault
  Page miss
  Page skip
- 24. 16. Data are transferred from cache memory to CPU in the units of



## 25. 17. If 'h' is the hit then (1-h) is

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hit ratio

🔵 miss ratio

hit rate

26. 18. Which of the following is the correct order of levels of memory in terms of increasing cost?

## Mark only one oval.

Registeràcache memory à main memoryàsecondary memory

Registerà main memory à cache memory àsecondary memory

Secondary memory àmain memoryà cache memoryà Registe

Secondary memory à cache memoryà main memoryà Register

27. 19. Registers are ...... speed storage devices.

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low

high

- \_\_\_\_ medium
- None of these

28. 20. Which address belongs to RAM?

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physical address

- absolute address
- logical address
- \_\_\_\_\_ relative address
- 29. 21. Least Recently used is a ...... algorithm.

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- 🔵 overwrite
- 30. 22. A register used to hold the instruction being executed is



31. 23. Which of the following stores the information only till power supply?

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32. 24. Which of the following stores the information in the form of electric charges?

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- SRAM RAM DRAM Cache
- 33. 25. The property where nearby data are accessed?

Mark only one oval.

\_\_\_\_ temporal

sequential

34. 26.Run time mapping from virtual to physical address is done by

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$\bigcirc$	Memory management unit
$\bigcirc$	CPU
$\bigcirc$	PC
$\bigcirc$	None of these

35. 27. DRAM is used as main memory as it

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- consumes less power
- 🔵 has high speed
- has lower cell density
- needs refreshing circuitry
- 36. 28. Cache memory acts between\_\_\_\_\_

- CPU and RAM
- CPU and registers
- RAM and ROM
- None of these

## 37. 29.Which of the following has smallest capacity

Mark only one oval.

$\bigcirc$	cache memory
$\bigcirc$	RAM
$\bigcirc$	secondary memory
$\bigcirc$	registers

38. 30.How many address lines are needed to address each memory locations in a 2048 x 4 memory chip?

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- 10
  11
  8
  12
- 39. 31.A register capable of shifting its binary information either to the right or the left is called a

- \_\_\_\_ parallel register
- serial register
- shift register
- 🔵 storage register

## 40. 32. Which of the following has largest capacity

Mark only one oval.

cache memory
 RAM
 secondary memory

registers

41. 33.Which memory unit has lowest access time?

Mark only one oval.

Registers

main memory

\_\_\_\_ magnetic disk

42. 34. The memory unit that communicates directly with the CPU is called the

Mark only one oval.

main memory

Secondary memory

shared memory

auxiliary memory

43. 35. The access time of memory is ..... the time required for performing any single CPU operation:

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- Shorter than
- Negligible than
- 🔵 Same as
- \_\_\_\_ Longer than
- 44. 36.The algorithm to remove and place new contents into the cache is called

Mark only one oval.

Rene	wal algorithm
------	---------------

- Replacement algorithm
- Mapping algorithm
- None of these
- 45. 37. If the searched data is found in the desired memory, it is said to be

- 🔵 hit ratio
- miss
- \_\_\_\_ hit
- hit rate

#### 46. 38..... is used to represent segment utilization as a function of time in pipelining.

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🔵 Block diagram

- 📃 Time diagram
- Space time diagram
- 🔵 Space diagram
- 47. 39. Data hazards occurs when

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- Greater performance loss
- Machine size is limited
- Some functional unit is not fully pipelined
- Pipeline changes the order of read/write access to operands
- 48. 40.Total number of clock cycles in pipelining is given by...... (where n = number of instruction and k = number of stages)

- \_\_\_\_\_ k-n-1
- \_\_\_\_\_ k+n-1
- \_\_\_\_\_ k-n+1
- \_\_\_\_\_ k+n+1

49. 41. Arithmetic Logic Unit (ALU) is used in computer for performing

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arithmetic operations

- logical operations
- Both of these
- none of these
- 50. 42. Which of the following is/are type of pipelining?

Mark only one oval.

- instruction
- Both of these
- none of these
- 51. 43. Which of the following is/are pipeline hazards?

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controldataresource

All of these

52. 44.A computer system with more than one number of processors is

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\_\_\_\_ multi-processor

- \_\_\_\_ multi-system
- \_\_\_\_ multi-computer
- \_\_\_\_ multi-group
- 53. 45. The mapping technique which stores three words with different tag but with same index is

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- 2 way set associative
- 1 way set associative
- 3 way set associative
- 4 way set associative
- 54. 46. MISD stands for

- Multiple instruction single data
- Memory instruction single data
- Multiple instruction sequence data
- Multiple information single data

55. 47. Array processor is related to which of the following classification?

Mark only one oval.

SIMD

- SISD
- MISD
- 56. 48. SISD stands for

Mark only one oval.

- Single instruction single data
- Single information single data
- Sequence instruction single data
- Single instruction sequence data
- 57. 49. Data hazards occur when

- Greater performance loss
- Machine size is limited
- Some functional unit is not fully pipelined
- Pipeline changes the order of read/write access to operands

# 58. 50.The sequence of operations performed by CPU in processing an instruction is

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$\square$	$\bigcirc$	Execution	cycle
_	_		

- Fetch cycle
- \_\_\_\_ Decode
- Instruction cycle
- 59. 51. The step during which a new instruction is read from the memory

Mark only one oval.

$\bigcirc$	Decode
$\bigcirc$	Fetch
$\bigcirc$	Execute
$\bigcirc$	none of these

60. 52. Each stage in pipelining generally completed within ...... cycle.

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61. 53. How many bits are required to represent addresses of data of cache memory with size 1K?

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62. 54. In DMA, the value of ...... register is decremented by one after each word transfer

# Mark only one oval.

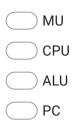
Control register
Address register
Word count register

- Buffer register
- 63. 55.Register which specifies the mode of transfer in DMA is

- Control register
- Address register
- Word count register
- Buffer register

## 64. 56. DMA controller transfer data without intervention of

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65. 57. Which of the following is/are type of control unit?

Mark only one oval.

$\bigcirc$	Hardwired
$\bigcirc$	Microprogrammed
$\bigcirc$	Both of these

- none of these
- 66. 58. BG signal in DMA stands for

- 🔵 bus give
- bus get
- bus grant
- buffer grant

67. 59.Interrupt initiated by I/O devices is called

Mark only one oval.

Software interrupt

- External interrupt
- Internal interru
- All of these
- 68. 60. When the CPU detects an interrupt, it then saves its:

Mark only one oval.

- Previous State
   Next State
   Both of these
- Current State
- 69. 61. A collection of four binary digits is called

Mark only one oval.

Byte

Character

Number

Nibble

70. 62. Peripheral devices are

Mark only one oval.

Internal devices

Any device

I/O devices

🔵 CPU

71. 63. When generating physical addresses from a logical address the offset is stored in \_\_\_\_\_

Mark only one oval.

Translation look-aside buffer

Relocation register

🔵 Page table

- Shift register
- 72. 64. The technique used to store programs larger than the memory is \_\_\_\_\_

Mark only one oval.

Overlays



Buffers

Both Extension registers and Buffers

# 73. 65. Does the Load instruction do the following operation/s?

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- Loads the contents of a disc onto a memory location
- Loads the contents of a location onto the accumulators
- Load the contents of the PCB onto the register
- None of these
- 74. 66. The BOOT sector files of the system are stored in \_\_\_\_\_

Mark only one oval.

_					
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	)	пa	IU	u١٤	δK

- ROM
- RAM
- Fast solid state chips in the motherboard
- 75. 67. Which of the following techniques used to effectively utilize main memory?

- Address binding
- Dynamic linking
- Dynamic loading
- Both Dynamic linking and loading

76. 68. The usual BUS structure used to connect the I/O devices is \_\_\_\_\_

Mark only one oval.

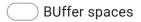
Star BUS structure

- Multiple BUS structure
- Single BUS structure
- Node to Node BUS structure
- 77. 69. The advantage of I/O mapped devices to memory mapped is \_\_\_\_\_

## Mark only one oval.

- The former offers faster transfer of data
- The devices connected using I/O mapping have a bigger buffer space
- The devices have to deal with fewer address lines
- No advantage as such
- 78. 70. To overcome the lag in the operating speeds of the I/O device and the processor we use \_\_\_\_\_

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- Status flags
- Interrupt signals
- Exceptions

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