# Online Examinations (Even Sem/Part-I/Part-II Examinations 2020 - 2021

Course Name - –Computer Organization and Architecture
Course Code -PCC-CS401

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Answer all the questions. Each question carry one mark.

9. 1.Which of the following is a universal logic gate?

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- [ ] XOR
- [ ] NOR
- [ ] OR
- [ ] XNOR

10. 2. Boolean algebra is also known as

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- Counting algebra
- Switching algebra
- Transistor algebra
- Gate algebra

11. 3. Which of the following is used to store intermediate result?

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- Accumulator
- MAR
- MDR
- Program Counter

12. 4. Which of the following is not a bus?____.

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- control bus
- data bus
- program bus
- address bus

13. 5. Which of the following is used to store the address of next instruction?

*Mark only one oval.*

- Accumulator
- MAR
- Program Counter
- MDR

14. 6.A collection of lines that connects several devices is called

*Mark only one oval.*

- peripheral connection wires
- bus
- Accumulator
- Internal wires

15. 7.The instructions like MOV or ADD are called as

*Mark only one oval.*

- OP-Code
- Commands
- Operators
- None of above

16. 8.In which addressing mode the address of the operand is specified?

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- Absolute
- Immediate
- Indirect
- Direct

17. 9. MRI indicates

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- Memory Reference Information
- Memory Reference Instruction
- Memory Registers Instruction
- Memory Register information

18. 10.Content addressable memory is also known as

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- Main memory
- Virtual memory
- Associative memory
- Auxiliary memory

19. 11. Memory management technique where allocated size is fixed -

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- paging
- segmentation
- fragmentation
- indexing

20. 12.Which of the following is/are type of multi processor on basis of memory?

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- Shared memory
- Distributed memory
- Both of these
- None of these

21. 13.Associative memory is ..... than RAM.

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- faster
- same
- slower
- does not depend

22. 14.Which of the following is/are the algorithm for page replacement?

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- FIFO
- LRU
- Optim
- All of these

23. 15. If the required page is not present in the main memory, it is said to be

*Mark only one oval.*

- Page hit
- Page fault
- Page miss
- Page skip

24. 16. Data are transferred from cache memory to CPU in the units of

*Mark only one oval.*

- blocks
- pages
- words
- bit

25. 17. If ‘h’ is the hit then (1-h) is

*Mark only one oval.*

- hit ratio
- miss
- miss ratio
- hit rate

26. 18. Which of the following is the correct order of levels of memory in terms of increasing cost?

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- Registeràcache memory à main memoryàsecondary memory
- Registerà main memory à cache memory àsecondary memory
- Secondary memory àmain memoryà cache memoryà Registe
- Secondary memory à cache memoryà main memoryà Register

27. 19. Registers are ..... speed storage devices.

*Mark only one oval.*

- low
- high
- medium
- None of these

28. 20. Which address belongs to RAM?

*Mark only one oval.*

- physical address
- absolute address
- logical address
- relative address

29. 21. Least Recently used is a ..... algorithm.

*Mark only one oval.*

- replacement
- delete
- renewal
- overwrite

30. 22. A register used to hold the instruction being executed is

*Mark only one oval.*

- IR
- MAR
- AC
- MDR

31. 23. Which of the following stores the information only till power supply?

*Mark only one oval.*

- SRAM
- RAM
- DRAM
- Cache

32. 24. Which of the following stores the information in the form of electric charges?

*Mark only one oval.*

- SRAM
- RAM
- DRAM
- Cache

33. 25. The property where nearby data are accessed?

*Mark only one oval.*

- temporal
- parallel
- spatial
- sequential

34. 26.Run time mapping from virtual to physical address is done by

*Mark only one oval.*

- Memory management unit
- CPU
- PC
- None of these

35. 27. DRAM is used as main memory as it

*Mark only one oval.*

- consumes less power
- has high speed
- has lower cell density
- needs refreshing circuitry

36. 28. Cache memory acts between_____

*Mark only one oval.*

- CPU and RAM
- CPU and registers
- RAM and ROM
- None of these

37. 29.Which of the following has smallest capacity

*Mark only one oval.*

- cache memory
- RAM
- secondary memory
- registers

38. 30.How many address lines are needed to address each memory locations in a 2048 x 4 memory chip?

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- 10
- 11
- 8
- 12

39. 31.A register capable of shifting its binary information either to the right or the left is called a

*Mark only one oval.*

- parallel register
- serial register
- shift register
- storage register

40. 32. Which of the following has largest capacity

*Mark only one oval.*

- cache memory
- RAM
- secondary memory
- registers

41. 33.Which memory unit has lowest access time?

*Mark only one oval.*

- Cache
- Registers
- main memory
- magnetic disk

42. 34. The memory unit that communicates directly with the CPU is called the

*Mark only one oval.*

- main memory
- Secondary memory
- shared memory
- auxiliary memory

43. 35. The access time of memory is ..... the time required for performing any single CPU operation:

*Mark only one oval.*

- Shorter than
- Negligible than
- Same as
- Longer than

44. 36.The algorithm to remove and place new contents into the cache is called

*Mark only one oval.*

- Renewal algorithm
- Replacement algorithm
- Mapping algorithm
- None of these

45. 37. If the searched data is found in the desired memory, it is said to be

*Mark only one oval.*

- hit ratio
- miss
- hit
- hit rate

46. 38……. is used to represent segment utilization as a function of time in pipelining.

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- Block diagram
- Time diagram
- Space time diagram
- Space diagram

47. 39. Data hazards occurs when

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- Greater performance loss
- Machine size is limited
- Some functional unit is not fully pipelined
- Pipeline changes the order of read/write access to operands

48. 40.Total number of clock cycles in pipelining is given by……. (where n = number of instruction and k = number of stages)

*Mark only one oval.*

- k-n-1
- k+n-1
- k-n+1
- k+n+1

49. 41. Arithmetic Logic Unit (ALU) is used in computer for performing

*Mark only one oval.*

- arithmetic operations
- logical operations
- Both of these
- none of these

50. 42.Which of the following is/are type of pipelining?

*Mark only one oval.*

- instruction
- arithmetic
- Both of these
- none of these

51. 43. Which of the following is/are pipeline hazards?

*Mark only one oval.*

- control
- data
- resource
- All of these

52. 44.A computer system with more than one number of processors is

*Mark only one oval.*

- multi-processor
- multi-system
- multi-computer
- multi-group

53. 45. The mapping technique which stores three words with different tag but with same index is

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- 2 way set associative
- 1 way set associative
- 3 way set associative
- 4 way set associative

54. 46. MISD stands for

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- Multiple instruction single data
- Memory instruction single data
- Multiple instruction sequence data
- Multiple information single data

55. 47. Array processor is related to which of the following classification?

*Mark only one oval.*

- SIMD
- SISD
- MISD
- MIMD

56. 48. SISD stands for

*Mark only one oval.*

- Single instruction single data
- Single information single data
- Sequence instruction single data
- Single instruction sequence data

57. 49. Data hazards occur when

*Mark only one oval.*

- Greater performance loss
- Machine size is limited
- Some functional unit is not fully pipelined
- Pipeline changes the order of read/write access to operands

58. 50.The sequence of operations performed by CPU in processing an instruction is

*Mark only one oval.*

- Execution cycle
- Fetch cycle
- Decode
- Instruction cycle

59. 51. The step during which a new instruction is read from the memory

*Mark only one oval.*

- Decode
- Fetch
- Execute
- none of these

60. 52. Each stage in pipelining generally completed within ..... cycle.

*Mark only one oval.*

- 1
- 2
- 3
- 4

61. 53.How many bits are required to represent addresses of data of cache memory with size 1K?

*Mark only one oval.*

- 10
- 9
- 8
- 11

62. 54. In DMA, the value of ..... register is decremented by one after each word transfer

*Mark only one oval.*

- Control register
- Address register
- Word count register
- Buffer register

63. 55.Register which specifies the mode of transfer in DMA is

*Mark only one oval.*

- Control register
- Address register
- Word count register
- Buffer register

64. 56. DMA controller transfer data without intervention of

*Mark only one oval.*

- MU
- CPU
- ALU
- PC

65. 57. Which of the following is/are type of control unit?

*Mark only one oval.*

- Hardwired
- Microprogrammed
- Both of these
- none of these

66. 58. BG signal in DMA stands for

*Mark only one oval.*

- bus give
- bus get
- bus grant
- buffer grant

67. 59.Interrupt initiated by I/O devices is called

*Mark only one oval.*

- Software interrupt
- External interrupt
- Internal interru
- All of these

68. 60.When the CPU detects an interrupt, it then saves its:

*Mark only one oval.*

- Previous State
- Next State
- Both of these
- Current State