Online Examinations (Even Sem/Part-I/Part-II Examinations 2020 - 2021

Course Name - –Microprocessor and Microcontroller
Course Code - BCA403

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Answer all the questions. Each question carry one mark.

9.   1. Why 8085 processor is called an 8 bit processor?

Mark only one oval.

◯ because 8085 processor has 8 bit ALU

◯ because 8085 processor has 8 bit data bus

◯ because 8085 processor has 16 bit data bus

◯ because 8085 processor has 16 bit address bus

10. 2. A microprocessor is a

Mark only one oval.

- ◯ SSI device
- ◯ MSI device
- ◯ LSI device
- ◯ VLSI device

11. 3. The microprocessor was introduced in the year

Mark only one oval.

- ◯ 1940
- ◯ 1971
- ◯ 1973
- ◯ 1980

12. 4. 8085 microprocessor has how many pins

Mark only one oval.

- ◯ 40
- ◯ 39
- ◯ 42
- ◯ 20

13.   5. The number of output pins in 8085 microprocessors are

Mark only one oval.

⬭ 27

⬭ 40

⬭ 19

⬭ 28

14.   6. Which of the following microprocessors is a 4 bit microprocessor?

Mark only one oval.

⬭ 4004

⬭ 8080

⬭ 8085

⬭ 8086

15.   7. Which pin is used for demultiplexing of address and data bus of 8085
       microprocessor?

Mark only one oval.

⬭ TRAP

⬭ ALE

⬭ IO/M´

⬭ READY

16.　8. In a computer where microprocessor is used as CPU is known as

Mark only one oval.

◯ Microprocessor

◯ Micro-computer

◯ Microcontroller

◯ All of these

17.　9. Intel 8085A microprocessor ALE signal is made high to

Mark only one oval.

◯ Enable the data bus to be used as low order address bus

◯ To latch data D0-D7 from data bus

◯ To disable data bus

◯ To achieve all the functions listed above

18.　10. An 8-bit microprocessor has an

Mark only one oval.

◯ 8 bit data bus

◯ 8-bit address bus

◯ 8-bit control bus

◯ 8-bit interrupt lines

19. 11. In an intel 8085A microprocessor, why is READY signal used?

Mark only one oval.

○ To indicate to user that the microprocessor is working and is ready for use

○ To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device.

○ To slow down a fast peripheral device so as to communicate at the microprocessor's device

○ None of the above

20. 12. Which of the following statements for Intel 8085 is correct?

Mark only one oval.

○ Program Counter (PC) specifies the address of the instruction last executed

○ PC specifies the address of the instruction being executed

○ PC specifies the address of the instruction to be executed

○ PC specifies the number of instructions executed so far

21. 13. In 8085 name of the 16 bit registers is

Mark only one oval.

○ stack pointer

○ program counter

○ Stack pointer and program counter

○ none of these

22. 14. The word size of 8085 microprocessor is

Mark only one oval.

◯ 8-bits

◯ 16-bits

◯ 20-bits

◯ 4-bits

23. 15. Both the ALU and control section of CPU employ which special purpose storage location?

Mark only one oval.

◯ Buffers

◯ Decoders

◯ Accumulators

◯ Registers

24. 16. How many times will the following loop be executed? XRA A MVI C, 05H LOOP; DCRC JNZ LOOP

Mark only one oval.

◯ once

◯ five

◯ infinite times

◯ four times

25.   17. The address bus of microprocessor is

Mark only one oval.

◯ unidirectional

◯ bi-directional

◯ unidirectional as well as bi-directional

◯ none of these

26.   18. The address / data bus in 8085 is _____.

Mark only one oval.

◯ multiplexed

◯ demultiplexed

◯ decoded

◯ encoded

27.   19. What does microprocessor speed depends on?

Mark only one oval.

◯ Clock

◯ Data bus width

◯ Address bus width

◯ Control bus width

28.   20. In 8085 microprocessor, for execution of the instruction DCX Rp (Rp is register pair) how many T-states are required?

Mark only one oval.

⬭ 6

⬭ 4

⬭ 3

⬭ 1

29.   21. After execution of instruction RRC, which one of the following flag will be affected

Mark only one oval.

⬭ Auxiliary Flag

⬭ Zero Flag

⬭ Sign Flag

⬭ Carry Flag

30.   22. The CALL location for TRAP is

Mark only one oval.

⬭ 0023H

⬭ 0032H

⬭ 0042H

⬭ 0024H

31.   23. Number of software interrupts supported by 8085 microprocessor is

Mark only one oval.

    ⬭ 7

    ⬭ 5

    ⬭ 8

    ⬭ 9

32.   24. When CALL instruction is executed, the SP will be

Mark only one oval.

    ⬭ SP-1

    ⬭ SP+1

    ⬭ SP-2

    ⬭ SP+2

33.   25. The number of T-States required for PCHL instruction execution is

Mark only one oval.

    ⬭ 4

    ⬭ 6

    ⬭ 8

    ⬭ 10

34.   26. In 8085 microprocessor, the RST6 instruction transfer Programme execution to
       following location

Mark only one oval.

⬭ 0030H.

⬭ 0032H.

⬭ 0048H.

⬭ 0024H.

35.   27. XCHG is an

Mark only one oval.

⬭ data transfer instruction

⬭ logical instruction

⬭ arithmatic instruction

⬭ none of these

36.   28. What is meant by maskable interrupts?

Mark only one oval.

⬭ an interrupt which can never be turned off

⬭ an interrupt that can be turned off by the programmer

⬭ an interrupt which can never be turned on

⬭ an interrupt which can never be turned on or off

37.   29. Which of the following instruction is not possible in 8085?

Mark only one oval.

⬭ POP PSW

⬭ POP B

⬭ POP D

⬭ POP 30 H

38.   30. How many T-states are required for execution of OUT 80H instruction?

Mark only one oval.

⬭ 10

⬭ 13

⬭ 16

⬭ 7

39.   31. Which interrupt has the highest priority?

Mark only one oval.

⬭ INTR

⬭ TRAP

⬭ RST6.5

⬭ RST6.6

40.　　32. What are level Triggering interrupts?

Mark only one oval.

◯ INTR & TRAP

◯ RST6.5 & RST5.5

◯ RST7.5 & RST6.5

◯ RST2.5 & RST6.2

41.　　33. Which interrupt is not level sensitive in 8085?

Mark only one oval.

◯ RST 6.5

◯ RST 7.5

◯ RST 5.5

◯ RST 4.5

42.　　34. What are software interrupts?

Mark only one oval.

◯ RST 0-7

◯ RST 5.5 - 7.5

◯ INTR, TRAP

◯ RST 4.4 - 6.4

43.   35. MOV A, C is an instruction of

Mark only one oval.

    ◯ One byte

    ◯ two byte

    ◯ three byte

    ◯ four byte

44.   36. LXI H, 2500 H is an instruction of

Mark only one oval.

    ◯ direct addressing mode

    ◯ indirect addressing mode

    ◯ register addressing mode

    ◯ Immediate addressing mode

45.   37. MVI A, 58H is an instruction of

Mark only one oval.

    ◯ direct addressing mode

    ◯ indirect addressing mode

    ◯ register addressing mode

    ◯ Immediate addressing mode

46.   38. During IO operation the IO/M ´ signal will be

Mark only one oval.

◯ LOW

◯ Tristate

◯ HIGH

◯ None of these

47.   39. By issuing which one of the following signal, CPU releases the system bus to
       DMA controller?

Mark only one oval.

◯ HOLD

◯ HLDA

◯ ALE

◯ READY

48.   40. The technique of assigning a memory address to each I/O device in the
       computer system is called:

Mark only one oval.

◯ memory-mapped I/O

◯ ported I/O

◯ dedicated I/O

◯ wired I/O

49.   41. 8086 has

Mark only one oval.

◯ 16 bit data bus and 20 bit address bus

◯ 8 bit data bus and 20 bit address bus

◯ 16 bit data bus and 16 bit address bus

◯ 8 bit data bus and 16 bit address bus

50.   42. The Microcontroller 8051 is

Mark only one oval.

◯ 8-bit processor

◯ 16-bit processor

◯ 32-bit processor

◯ 64-bit processor

51.   43. Which of the following instruction is a logical instruction?

Mark only one oval.

◯ DIV AB

◯ TEST

◯ CALL

◯ AAM

52.   44. How many register banks are present in 8051 microcontroller?

Mark only one oval.

○ 4

○ 3

○ 2

○ 1

53.   45. 8051 series of microcontrollers are made by which of the following companies?

Mark only one oval.

○ Atmel

○ Philips

○ Atmel & Philips

○ None of the mentioned

54.   46. AT89C2051 has RAM of:

Mark only one oval.

○ 128 bytes

○ 256 bytes

○ 64 bytes

○ 512 bytes

55.　47. When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected?

Mark only one oval.

- ( ) PSW
- ( ) SP
- ( ) DPTR
- ( ) PC

56.　48. Which of the following comes under the indexed addressing mode?

Mark only one oval.

- ( ) MOVX A, @DPTR
- ( ) MOVC @A+DPTR,A
- ( ) MOV A,R0
- ( ) MOV @R0,A

57.　49. Which instruction is used to check the status of a single bit?

Mark only one oval.

- ( ) MOV A,P0
- ( ) ADD A,#05H
- ( ) JNB P0.0, label
- ( ) CLR P0.05H

58.   50. Which of the following registers are not bit addressable?

Mark only one oval.

◯ SCON

◯ PCON

◯ A

◯ PSW

59.   51. How many bytes of bit addressable memory is present in 8051 based microcontrollers?

Mark only one oval.

◯ 8 bytes

◯ 32 bytes

◯ 16 bytes

◯ 128 bytes

60.   52. When 8051 wakes up then 0x00 is loaded to which register?

Mark only one oval.

◯ DPTR

◯ SP

◯ PC

◯ PSW

61.   53. A microcontroller at-least should consist of

Mark only one oval.

⬭ RAM, ROM, I/O devices, serial and parallel ports and timers

⬭ CPU, RAM, I/O devices, serial and parallel ports and timers

⬭ CPU, RAM, ROM, I/O devices, serial and parallel ports and timers

⬭ CPU, ROM, I/O devices and timers

62.   54. Which of the following are 16 bit register in 8051 microcontroller?

Mark only one oval.

⬭ DPTR

⬭ IE

⬭ TMOD

⬭ PC

63.   55. Which of the following register can be used as two individual 8 bit register in 8051?

Mark only one oval.

⬭ DPTR

⬭ PC

⬭ SBUF

⬭ PSW

64.   56. In 8051 which interrupt has highest priority?

Mark only one oval.

⬭ IE1

⬭ TF0

⬭ IE0

⬭ TF1

65.   57. The 8051 microcontroller is of ___pin package as a _____ processor.

Mark only one oval.

⬭ 30, 1byte

⬭ 20, 1 byte

⬭ 40, 8 bit

⬭ 40, 8 byte

66.   58. On power up, the 8051 uses which RAM locations for register R0– R7

Mark only one oval.

⬭ 00-2F

⬭ 00-07

⬭ 00-7F

⬭ 00-0F

67.　59. JZ, JNZ, DJNZ, JC, JNC instructions monitor the bits of which register in 8051?

Mark only one oval.

○ DPTR

○ B

○ A

○ PSW

68.　60. Which of the following instruction is incorrect?

Mark only one oval.

○ CPL A

○ SWAP A

○ CLR C

○ RL B

69.　61. Consider the following registers: a. Accumulator and flag register b. B and C register c. D and E register d. H and L register Which of these 8-bit registers of 8085 microprocessor can be paired together to make a 16-bit register?

Mark only one oval.

○ a,c,d

○ b,c,d

○ a,b,d

○ a,b,c

70.   62. What is RIM in context of microprocessor?

Mark only one oval.

◯ Ready Interrupt Mask

◯ Reading Interrupt Mask

◯ Read Interrupt Mask

◯ Read Integer Mask

71.   63. STA 8500H is executed by

Mark only one oval.

◯ one machine cycle

◯ two machine cycle

◯ three machine cycle

◯ four machine cycle

72.   64. OUT 02H is executed by

Mark only one oval.

◯ one machine cycle

◯ two machine cycle

◯ three machine cycle

◯ four machine cycle

73.   65. IN 00H is an instruction of

Mark only one oval.

⬭ direct addressing mode

⬭ indirect addressing mode

⬭ register addressing mode

⬭ Immediate addressing mode

74.   66. ADD B is executed by

Mark only one oval.

⬭ one machine cycle

⬭ two machine cycle

⬭ three machine cycle

⬭ four machine cycle

75.   67. LDAX D is an instruction of

Mark only one oval.

⬭ direct addressing mode

⬭ indirect addressing mode

⬭ register addressing mode

⬭ Immediate addressing mode

76.   68. LHLD 2500H is an instruction of

Mark only one oval.

- ( ) direct addressing mode
- ( ) indirect addressing mode
- ( ) register addressing mode
- ( ) Immediate addressing mode

77.   69. ADI, 01 H is an instruction of

Mark only one oval.

- ( ) direct addressing mode
- ( ) indirect addressing mode
- ( ) register addressing mode
- ( ) Immediate addressing mode

78.   70. CMP B is an instruction of

Mark only one oval.

- ( ) direct addressing mode
- ( ) indirect addressing mode
- ( ) register addressing mode
- ( ) Immediate addressing mode

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