Online Examinations (Even Sem/Part-I/Part-II Examinations 2020 - 2021

Course Name - –VLSI Devices and Design
Course Code - PCC-EC603

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Answer all the questions. Each question carry one mark.

9. 1. Moore was co-founder of

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- TCS
- Infosys
- Intel
- Wipro

10. 2. Medium scale integration has _____ logic gates.

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- 13 to 99
- 1 to 12
- 100 to 9,999
- 10,000 to 99,999

11. 3. As die size shrinks, the complexity of making the photomasks _____

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- increases
- decreases
- remains the same
- cannot be determined

12. 4. What is the design flow of VLSI system? i. architecture design ii. circuit design iii. logic design iv. physical design

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- ii-i-iii-iv
- iv-i-iii-ii
- iii-ii-i-iv
- i-iii-ii-iv

13. 5. Which is the high level representation of VLSI design?

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- architect design
- logic design
- circuit design
- physical design

14. 6. Gate minimization technique is used to simplify the logic.

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- true
- false
- In the case of Silicon, even if the number of the gate is minimised, logic will not be simplified
- In the case of Ge, even if the number of the gate is minimised, logic will not be simplified

15. 7. nMOS fabrication process is carried out in _____

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- thin wafer of a single crystal
- thin wafer of multiple crystals
- thick wafer of a single crystal
- thick wafer of a multiple crystal

16. 8. What kind of layer is provided upon which other layers may be deposited and patterned.

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- insulating
- conducting
- silicon
- semiconducting

17. 9. In nMOS device, gate material could be _____

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- silicon
- polysilicon
- boron
- phosphorus

18. 10. Electronics are characterized by _____

Mark only one oval.

- low cost
- low weight and volume
- reliability
- low cost, low weight and volume, reliability

19. 11. nMOS devices are formed in _____

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- p-type substrate of high doping level
- n-type substrate of low doping level
- p-type substrate of moderate doping level
- n-type substrate of high doping level

20. 12. Source and drain in nMOS device are isolated by _____

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- a single diode
- two diodes
- three diodes
- four diodes

21. 13. What is the condition for non saturated region?

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- Vds = Vgs – Vt
- Vgs lesser than Vt
- Vds lesser than Vgs – Vt
- Vds greater than Vgs – Vt

22. 14. What is the condition for non conducting mode?

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- Vds lesser than Vgs
- Vgs lesser than Vds
- Vgs = Vds = 0
- Vgs = Vds = Vs = 0

23. 15. MOS transistor structure is _____

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- symmetrical
- non symmetrical
- semi symmetrical
- pseudo symmetrical

24. 16. Which is the commonly used bulk substrate in nMOS fabrication?

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- either bulk silicon or silicon-on-sapphire
- silicon-di-oxide
- aluminium
- copper

25. 17. Contact cuts are made in _____

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- only source
- only drain
- source, drain and gate
- diffusion layer

26. 18. Sllicon-di-oxide is a good insulator.

Mark only one oval.

- True
- False
- Sometimes
- Never

27. 19. In nMOS, _____ is used to suppress unwanted conduction.

Mark only one oval.

- phosphorus
- boron
- silicon
- oxygen

28. 20. The FPGA refers to _____

Mark only one oval.

- First programmable Gate Array
- Field Programmable Gate Array
- First Program Gate Array
- Field Program Gate Array

29. 21. In which design, all circuitry and all interconnections are designed?

Mark only one oval.

- full custom design
- semi-custom design
- gate array design
- transistor design

30. 22. In which method regularity is used to reduce complexity?

Mark only one oval.

- random approach
- hierarchical approach
- algorithmic approach
- semi-design approach

31. 23. Which design is faster?

Mark only one oval.

- full custom design
- semi-custom design
- gate array design
- transistor design

32. 24. Which type of simulation mode is used to check the timing performance of a design?

Mark only one oval.

- Behavioural
- Switch-level
- Transistor-level
- Gate-level

33. 25. Which type of device FPGA is?

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- SLD
- SROM
- EPROM
- PLD

34. 26. In FPGA, vertical and horizontal directions are separated by _____

Mark only one oval.

- A line
- A channel
- A strobe
- A flip-flop

35. 27. The inputs in the PLD is given through _____

Mark only one oval.

- NAND gates
- OR gates
- NOR gates
- AND gates

36. 28. The n-type semiconductor have _____ as majority carriers.

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- Holes
- Negative ions
- Electrons
- Positive ions

37. 29. The majority carriers of p-type semiconductor are:

Mark only one oval.

- Holes
- Negative ions
- Electrons
- Positive ions

38. 30. The n-MOS transistor is made up of:

Mark only one oval.

- N-type source, n-type drain and p-type bulk
- N-type source, p-type drain and p-type bulk
- P-type source, n-type drain and n-type bulk
- P- type source, p-type drain and n-type bulk

39. 31. The drain current is varied by:

Mark only one oval.

- Gate to source voltage
- Gate current
- Source Voltage
- None of the mentioned

40. 32. The n-MOSFET is working as accumulation mode when:

Mark only one oval.

- Gate is applied with positive voltage
- Gate is grounded
- Gate is applied with a negative voltage
- Gate is connected to the source

41. 33. Which MOSFET is generally grounded in a circuit?

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- PMOS
- NMOS
- CMOS
- DMOS

42. 34. The current through the n-MOS transistor will flow when:

Mark only one oval.

- Vgs > Vtreshold, Vds=0
- Vgd < Vtreshold, Vds=0
- Vgs > Vtreshold, Vds>0
- Vgd > Vtreshold, Vds<0

43. 35. The conduction of current IDS depends on: i) Gate to source voltage ii) Drain to source voltage iii) Bulk to source voltage iv) Threshold voltage v) Dimensions of MOSFET

Mark only one oval.

- Only i
- Only i, ii and iii
- Only v
- All of the mentioned

44. 36. If the n-MOS and p-MOS of the CMOS inverters are interchanged the output is measured at:

Mark only one oval.

- Source of both transistor
- Drains of both transistor
- Drain of n-MOS and source of p-MOS
- Source of n-MOS and drain of p-MOS

45. 37. What will be the effect on output voltage if the positions of n-MOS and p-MOS in CMOS inverter circuit are exchanged?

Mark only one oval.

- Output is same
- Output is reversed
- Output is always high
- Output is always low

46. 38. The CMOS inverter consists of:

Mark only one oval.

- Enhancement mode n-MOS transistor and depletion mode p-MOS transistor
- Enhancement mode p-MOS transistor and depletion mode n-MOS transistor
- Enhancement mode p-MOS transistor and enhancement mode p-MOS transistor
- Enhancement mode p-MOS transistor and enhancement mode n-MOS transistor

47. 39. When the input of the CMOS inverter is equal to Inverter Threshold Voltage Vth, the transistors are operating in:

Mark only one oval.

- N-MOS is cutoff, p-MOS is in Saturation
- P-MOS is cutoff, n-MOS is in Saturation
- Both the transistors are in linear region
- Both the transistors are in saturation region

48. 40. Which of these invertors is more efficient?

Mark only one oval.

- Depletion mode n-MOS inverter
- pMOS inverter
- CMOS inverter
- Resistive load nMOS inverter

49. 41. The Fermi potential is the function of:

Mark only one oval.

- ◯ Temperature
- ◯ Doping concentration
- ◯ Difference between Fermi level and intrinsic Fermi level
- ◯ All of the mentioned

50. 42. In positive logic convention, the true state is represented as:

Mark only one oval.

- ◯ 1
- ◯ 0
- ◯ -1
- ◯ -0

51. 43. In CMOS logic circuit, the switching operation occurs because:

Mark only one oval.

- ◯ Both n-MOSFET and p-MOSFET turn OFF simultaneously for input '0' and turn ON simultaneously for input '1'
- ◯ Both n-MOSFET and p-MOSFET turn ON simultaneously for input '0' and turn OFF simultaneously for input '1'
- ◯ N-MOSFET transistor turns ON, and p-MOSFET transistor turns OFF for input '1' and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input '0'
- ◯ None of the mentioned

52. 44. When both nMOS and pMOS transistors of CMOS logic gates are ON, the output is:

Mark only one oval.

- 1 or Vdd or HIGH state
- 0 or ground or LOW state
- Crowbarred or Contention(X)
- None of the mentioned

53. 45. Total number of inputs in a half adder is _____

Mark only one oval.

- 2
- 3
- 4
- 1

54. 46. If A and B are the inputs of a half adder, the sum is given by _____

Mark only one oval.

- A AND B
- A OR B
- A XOR B
- A EX-NOR B

55. 47. Half-adders have a major limitation in that they cannot _____

Mark only one oval.

- Accept a carry bit from a present stage
- Accept a carry bit from a next stage
- Accept a carry bit from a previous stage
- Accept a carry bit from the following stages

56. 48. If A, B and C are the inputs of a full adder then the sum is given by _____

Mark only one oval.

- A AND B AND C
- A OR B AND C
- A XOR B XOR C
- A OR B OR C

57. 49. How many AND, OR and EXOR gates are required for the configuration of full adder?

Mark only one oval.

- 1, 2, 2
- 2, 1, 2
- 3, 1, 2
- 4, 0, 1

58. 50. Latch is a device with _____

Mark only one oval.

- One stable state
- Two stable state
- Three stable state
- Infinite stable states

59. 51. Two stable states of latches are _____

Mark only one oval.

- Astable & Monostable
- Low input & high output
- High output & low output
- Low output & high input

60. 52. The full form of SR is _____

Mark only one oval.

- System rated
- Set reset
- Set ready
- Set Rated

61. 53. The outputs of SR latch are _____

Mark only one oval.

- x and y
- a and b
- s and r
- q and q'

62. 54. CMOS technology is used in developing which of the following?

Mark only one oval.

- microprocessors
- microcontrollers
- digital logic circuits
- all of the mentioned

63. 55. In CMOS fabrication, nMOS and pMOS are integrated into the same substrate.

Mark only one oval.

- true
- false
- can't be determined
- sometimes true sometimes false

64. 56. Oxidation process is carried out using _____

Mark only one oval.

- high purity oxygen
- low purity oxygen
- sulphur
- nitrogen

65. 57. In CMOS fabrication, the photoresist layer is exposed to _____

Mark only one oval.

- visible light
- ultraviolet light
- infrared light
- fluorescent

66. 58. P-well doping concentration and depth will affect the _____

Mark only one oval.

- threshold voltage
- Vss
- Vdd
- Vgs

67. 59. N-well is formed by _____

Mark only one oval.

- decomposition
- diffusion
- dispersion
- filtering

68. 60. Which statement is false concerning Moore's Law?

Mark only one oval.

- The term was named for Gordon Moore.
- Gordon Moore was one of the founders of IBM.
- In the 1960s the storage density of integrated circuits on a silicon chip doubled about every year.
- Today, when we speak of Moore's Law we refer to the doubling of computer power every 18 months.

69. 61. How many gates per chip are used in first-generation Integrated Circuits?

Mark only one oval.

- 3-30
- 30-300
- 300-3000
- More than 3000

70. 62. MOS transistors consist of which of the following?

Mark only one oval.

- semiconductor layer
- metal layer
- layer of silicon-di-oxide
- all of the mentioned

71. 63. The gate region of transistor does not consist of _____

Mark only one oval.

- semiconductor layer
- insulating layer
- metal layer
- ground layer

72. 64. In N channel MOSFET which is the more negative of the elements?

Mark only one oval.

- source
- gate
- drain
- source and drain

73. 65. Enhancement mode device acts as ____ switch, depletion mode acts as _____ switch.

Mark only one oval.

- open, closed
- closed, open
- open, open
- close, close

74. 66. In P channel MOSFET which is the more positive of the elements?

Mark only one oval.

- a. source
- b. gate
- c. drain
- d. source and drain

75. 67. In the inverter circuit, the output is taken from which part of nMOS and pMOS?

Mark only one oval.

- source - source
- drain - drain
- source - drain
- drain - source

76. 68. Which component is added to the p-type material in order to get the impurity concentration in epitaxial films?

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- Bi-borane (B2H2)
- Phosphine (PH3)
- Boron chloride (BCl3)
- Phosphorous pentoxide (P2O5)

77. 69. Which of the following is used to obtain silicon crystal structure while fabricating Integrating Circuits?

Mark only one oval.

- Oxidation
- Epitaxial growth
- Photolithography
- Glass wafer preparations

78. 70. For oxidation process, silicon wafers are heated to a high temperature and simultaneously they are exposed to a gas containing _____

Mark only one oval.

- H2O
- Si
- N2
- H2

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