

Online Assessment (Even Sem/Part-I/Part-II Examinations 2019 - 2020)

Course Name - Microprocessor and Microcontroller

Course Code - BCA404A/BCS404A/BHN401A

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Answer all the questions. Each question carry one mark.

9. 1. The word size of 8085 microprocessor is

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- 8-bits
- 16-bits
- 20-bits
- 4-bits

10. 2. Both the ALU and control section of CPU employ which special purpose storage location?

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- Buffers
- Decoders
- Accumulators
- Registers

11. 3. Which stack is used in 8085?

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- FIFO
- LIFO
- FILO
- LILO

12. 4. Name of typical dedicated register is:

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- PC
- IR
- SP
- All of these

13. 5. The address bus of microprocessor is

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- unidirectional
- bi-directional
- unidirectional as well as bi-directional
- None of these

14. 6. A microprocessor performs as

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- CPU of a computer
- memory of a computer
- output device of a computer
- input device of a computer

15. 7. The 64 bit processor is

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- Pentium
- Pentium II
- Pentium III
- Pentium 4

16. 8. Consider the following I) Sign flag II) Trap flag III) Parity flag IV) Auxiliary carry flag Which one of the above flags is/are present in 8085 microprocessor?

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- (I) only
- (I) & (II)
- (II) & (III)
- (I) ,(III) & (IV)

17. 9. After add 89H & 79H , the status of Parity flag will be

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- 0
- 1
- X
- Unchanged

18. 10. What is the meaning of the instruction MVI A,05H?

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- data 05H is stored in the accumulator
- fifth bit of accumulator is set to one
- address 05H is stored in the accumulator
- none of the mentioned

19. 11. What is SIM?

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- Select Interrupt Mask
- Shoting Interrupt Mask
- Set Interrupt Mask
- None of these

20. 12. Let 81H & C2H are added. The RAR is executed. The content of the Accumulator will be

Mark only one oval.

- 82H
 87H
 90H
 97H

21. 13. HLT op-code means

Mark only one oval.

- Load data to accumulator
 Store result in memory
 Load accumulator with contents of register
 End of program

22. 14. Which instruction is required to rotate the content of accumulator one bit right along with carry?

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- RLC
 RAL
 RRC
 RAR

23. 15. STA 2070H is an instruction of

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- One byte
- two byte
- three byte
- four byte

24. 16. MOV A, B is an instruction of

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- direct addressing mode
- indirect addressing mode
- register addressing mode
- Immediate addressing mode

25. 17. XCHG is an

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- data transfer instruction
- arithmetic instruction
- logical instruction
- I/O and stack pointer instruction

26. 18. What is RIM in context of microprocessor?

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- Ready Interrupt Mask
- Reading Interrupt Mask
- Read Interrupt Mask
- Read Integer Mask

27. 19. A two byte instruction consists of

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- opcode and operand
- opcode only
- opcode and two operands
- operand only

28. 20. How many times will the following loop be executed? XRA A MVI C, 05H LOOP; DCRC JNZ LOOP

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- once
- five times
- infinite times
- depends on initial value of A

29. 21. How many address lines are required to access 1 MB RAM using microprocessor?

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- 16
- 8
- 20
- 12

30. 22. Which flags of 8086 are not present in 8085?

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- TF
- DF
- OF
- All of these

31. 23. What is the size of instruction Queue of 8086 microprocessor?

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- 3
- 5
- 6
- 8

32. 24. In 8086 microprocessor, the size of each segment is

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32 KB

64 KB

16 KB

8 KB

33. 25. The Intel 8086 microprocessor is a _____ processor.

Mark only one oval.

8 bit

16 bit

32 bit

4 bit

34. 26. The 16 bit flag of 8086 microprocessor is responsible to indicate _____.

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the condition of result of ALU operation

the condition of memory

the result of addition

the result of subtraction

35. 27. In 8086 the overflow flag is set when _____.

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- the sum is more than 16 bits
- signed numbers go out of their range after an arithmetic operation
- carry and sign flags are set
- subtraction

36. 28. In 8086 microprocessor the following has the highest priority among all type interrupts?

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- NMI
- DIV 0
- TYPE 255
- OVER FLOW

37. 29. In 8086 microprocessor one of the following statements is not true?

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- coprocessor is interfaced in max mode
- coprocessor is interfaced in min mode
- i/o can be interfaced in max / min mode
- supports pipelining

38. 30. 8088 microprocessor differs with 8086 microprocessor in _____.

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- data width on the output
 - address capability
 - support of coprocessor
 - support of MAX / MIN mode
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