BRAINWARE UNIVERSITY

Course – MCA

Computer Architecture and Microprocessor (MCA201 / MCA201(BL))

(Semester – 2)

Time allotted: 3 Hours   **Full Marks: 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Questions)   10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) The names of the 8-bit registers in 8085 microprocessor one
   1. SP   2. Accumulator
   3. Increment/Decrement Register   4. W
   a. 1 and 2 are correct   b. 2 and 4 are correct
   c. 1, 2 and 4 are correct   d. 2 , 3 and 4 are correct

(ii) The addressing mode of the instruction CMA is
   a. Direct addressing mode instruction   b. Indirect addressing mode instruction
   c. Implied addressing mode instruction   d. Immediate addressing mode instruction

(iii) The instruction LDAX R_p is (here, R_p is defining the register pair)
   a. One byte instruction   b. Two byte instruction
   c. Three byte instruction   d. None of these

(iv) The Accumulator of 8085 microprocessor contains the value 95_H. After execution of instruction ADI 80_H what will be the value of S and CY flag will be
   a. 0 and 1   b. 1 and 0
   c. Both are 0   d. None of these

(v) Consider a memory unit with capacity $4K \times 7$ bits, The number of address lines to indentify each word is
   a. 7   b. 256
   c. 12   d. 16

(vi)   The length of the address bus of 8085 microprocessor is

   a. 8   b. 16
   c. 32   d. 64

(vii)   In 8085 microprocessor, the instructions JMP and JPO are

   a. Conditional and unconditional   b. Unconditional and conditional jump
       jump respectively   respectively
   c. Both are conditional jump   d. Both are unconditional jump

(viii)   The interrupt having the highest priority is

   a. TRAP   b. RST 5.5
   c. RST 7.5   d. RST 6.5

(ix)   If the 8085 microprocessor the accumulator has 45_H and register B has 23_H. The content of the accumulator after execution of instruction XRA B will be.

   a. 66_H b. 77_H
   c. $3E_H$ d. 60_H

(x)   In 8085 microprocessor, for execution of the instruction XCHG, number of T-states e required is

   a. 4   b. 6
   c. 1   d. 3

Group – B

(Short Answer Type Questions)   3 x 5 = 15

Answer any *three* from the following

2. What do you mean by a machine cycle in a microprocessor?
    In 8085 microprocessor, the accumulator has 46_H. After execution of
    instruction ANI 96_H what will be the values of flags.   [2+3]

3. Write a program to evaluate the following arithmetic statement:
    B = (X * Z) - (Y * Z) using two and one address instructions.
    Where the X, Y, Z and U are memory locations.   [5]

4. A computer has 26-bit instructions and 10 bit addresses. If there are 56
    two-address instructions, how many one-address instructions can be
    formulated?   [5]

5. Specify the content of the accumulator and CY flag when the following
    instructions are executed:
                MVI A, $6D_H$
                CMA
                RRC
                RAL   [5]

6. Write an assembly language program in 8085 microprocessor to find the
    largest byte from a set of bytes.   [5]

Group – C

(Long Answer Type Questions)   3 x 15 = 45

Answer any *three* from the following

7.   (a)   Explain various addressing modes of 8085 microprocessor.   [8]
     (b)   What is flag register? Explain various flags of microprocessor 8085.   [7]

8.   (a)   Construct a $2K \times 8$ large RAM type memory with $1K \times 4$ RAM chips.   [10]
     (b)   Consider a memory chip of size $32K \times 8$. Find the length of the address bus and data bus to connect the memory chip with the CPU. To design the above memory chip how many Ram chips of size $8K \times 4$ is required.   [5]

9.   (a)   With a proper timing diagram explain the memory write machine cycle of 8085 microprocessor.   [10]
     (b)   If the clock frequency of 8085 microprocessor is 10 MHz, how much time is required to execute an instruction of 35 T-states?   [5]

10.   (a)   A digital computer has a common bus system for 16 registers of 4 bits each. The bus is constructed with multiplexers.
         (i)   How many selection inputs are there in the bus?
         (ii)   How many multiplexer are there in the bus?
         (iii)   What size of multiplexers is needed?   [2+4+4]
     (b)   What is the function of program counter and stack pointer? If the address bus of a microprocessor is 2N, then what will be the length of the program counter?   [4+1]

11.   (a)   In microprocessor 8085, explain the timing diagram for STA 30C1$_H$.   [15]