BRAINWARE UNIVERSITY

Course – BCA

Computer Architecture and Organization (BCA203 / BCAC203)

(Semester – 2)

Time allotted: 3 Hours **Full Marks : 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Questions) 10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) What is the outcome of an Effective addressing?

a. The information from which the memory address of the operand can be determined.

b. The operand or its address explicitly, to determine the address of an operand

c. A data. That defines the actual location of a memory element

d. A memory portion, that defines the recent addresses

(ii) What are the elementary components of a single DRAM cell?

a. Six transistors

b. Two transistors and one capacitor

c. Two transistors and two inverters

d. One transistor with a capacitor

(iii) What is the format of IEEE 754 single precision format?

a. 64-bit format in which 11-bit is for biased exponent E', 52-bit for mantissa M and 1-bit for the sign of the number.

b. 64-bit format in which 52 -bit is for biased exponent E', 11-bit for mantissa M and 1-bit for the sign of the number.

c. 32-bit format, in which 8-bit is for exponent, 23-bit is for mantissa, 1 bit to represent the sign bit

d. 32-bit format, in which 23-bit is for exponent, 8-bit is for mantissa, 1 bit to represent the sign bit

(iv) How many address buses and data buses are there for a RAM chip of size 1K X 8?

a. 10 bit address bus and 8 bit data bus
b. 8 bit data bus and 10 bit address bus
c. 1K bit address bus and 8 bit data bus
d. 1K bit data bis and 8 bit address bus

(v) How to measure the performance of a cache memory?

a. In terms of a quantity called 'hit ratio'
b. In terms of a quantity called 'miss ratio'
c. By a probability
d. In terms of locality of reference

(vi) What are the disadvantage of Optical disks over magnetic storages?

a. Optical disks are bigger in size
b. Optical disks have lower storage capacity.
c. Optical disks are expansive
d. Optical disks have slower seek-times and transfer rates than magnetic media

(vii) How Structural hazards may occur in pipeline?

a. Any situation where there is more than one pipeline
b. Any situation where there is not enough hardware is a structural hazard
c. Any situation where there is more hardware options
d. Any situation where there is no any pipeline procedure.

(viii) What is the function of a program control unit ?

a. It's function is to fetch instructions from memory and interrupt them
b. It's function is to fetch data from memory and use them
c. It's function is to fetch program from memory and process them
d. It's function is to count program and use them for the next process

(ix) What are the main advantages of associative memory?

a. Associative memory is cheap
b. It is suitable to store data rapidly
c. Associative memory is built with semiconductors
d. It is suitable for parallel searches due to its organization

(x) What are the uses of general purpose registers?

a. To store general input bits and intermediate data bits
b. To store data and intermediate results during the execution of a program
c. To store cache elements and hit ratio information
d. To store carry bits, and propagate the bits to carry flag register

Group – B

(Short Answer Type Questions) 3 x 5 = 15

Answer any *three* from the following

2. What are the advantages of having different addressing modes in a computer architecture? Explain Implied Mode and Immediate Mode with example. [3+2]

3. Why frequent refreshing is necessary for DRAM type memory? Describe a typical DRAM memory cell with necessary logic diagram. [2+3]

4. Compare various Lengths of Instructions through a proper arithmetic Expression. [5]

5. Compare Structural Hazards and Data Hazards with suitable examples. [5]

6. Explain step by step procedure for I/O Interface (Interrupt and DMA Mode) procedure. [5]

Group – C

(Long Answer Type Questions) 3 x 15 = 45

Answer any *three* from the following

7. (a) Construct a 1K X 16 large RAM type memory with 512 X 8 RAM chips. [10]

(b) Describe the working principle a typical CMOS SRAM type memory cell with necessary circuit diagram. [5]

8. (a) A memory sub system has with a hierarchical cache memory-main has cache access time of 60 nsec., main memory access time of 120 nsec. and an overall hit ratio of 0.12. Calculate efficiency of the memory system. [7]

   (b) A three level memory system having cache access time of 5 nsec, and disk access time of 40 nsec, it has a cache hit ratio of 0.96 and the main memory hit ratio of 0.9. what should be the main memory access time to achieve an overall access time of 16 nsec? [8]

9. (a) Show how the number of addresses affects a computer program? Evaluate the arithmetic statement X= (A+B) – (C+D) using zero, one, two or three address instructions. [8]

   (b) Represent decimal number 210.25_{10} in IEEE 754 floating point format. [7]

10. (a) Show the bus connection with a CPU to connect four RAMs of size 256 X 8 bits each and a ROM of size512 X 8 bit in size. Assume that the CPU has 8 bit data bus and 16 bit address bus [10]

    (b) Compare SRAM with DRAM [5]

11. Write short notes on any *three*

    (a) Optical storage vs Magnetic storage

    (b) Typical characteristics of RISC architecture

    (c) IAS computer and its organization of the CPU and main memory

    (d) Serial adder and its application

    (e) RISC and CISC [5+5+5]