# BRAINWARE UNIVERSITY

**Course – MCA**

**Computer Architecture & Microprocessor (MCA 201)**

(Semester – 2)

**Time allotted: 3 Hours** **Full Marks : 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

## Group –A

(Multiple Choice Type Questions) 10 x 1 = 10

1. Choose the correct alternative for the following : (*Any Ten*)

(i) Which register can interact with the secondary storage ?
(a) MAR (b) PC (c) IR (d) R0

(ii) The fastest data access is provided using
(a) Caches (b) DRAM's (c) SRAM's (d) Registers

(iii) A hard disk with 20 surfaces will have _____ heads.
(a) 10 (b) 5 (c) 1 (d) 20

(iv) The binary address issued to data or instructions is called as
(a) Physical address (b) Location
(c) Relocatable address (d) Logical address

(v) The DMA transfers performed by a control circuit is called
(a) Device interface (b) DMA controller
(c) Data controller (d) Overlooker

(vi) 8085 microprocessor operates at a frequency of
(a) 6 MHz (b) 3.2 MHz (c) 5 MHz (d) 3 MHz

(vii) READY is used for
(a) Input (b) Output (c) Both (a) and (b) (d) None of these

(viii) What is the vector call location of NMI?

(a) 002C H (b) 0028 H (c) 0010 H (d) 0024 H

(ix) RST 7.5 interrupt is

(a) Vectored & Maskable (b) Vectored & Non-Maskable

(c) Direct & Maskable (d) Direct & Non-Maskable

(x) If DMA request is sent to the microprocessor with a high signal to the HOLD pin, the microprocessor acknowledge the request

(a) after completing the present cycle (b) immediately after receiving the signal

(c) after completing the program (d) none of these

(xi) Select the invalid instruction

(a) MOV M, A (b) ADI 67 (c) LDAX B (d) STAX H

## Group – B

(Short Answer Type Question) 3 x 5 = 15

Answer any *three* from the following:

2. What do you mean by Feng's and Handlers's classification?

3. Describe the Harvard architecture.

4. Explain Static RAM.

5. Compare Demand Driven, Control Flow and Data Flow computers.

6. What do you mean by Boot Sequence?

## Group – C

(Long Answer Type Question) 3 x 15 = 45

Answer any *three* from the following:

7. (a) What are the special purpose registers available in Intel 8085A?

(b) Explain each of these special purpose registers [5 + 10]

8. (a) What is Flynn's classification?

(b) Explain each of the associated architecture with proper diagram. [5 + 10]

9. (a) Explain the Pipeline concept.

(b) Design a 1K X 4 RAM using 1K X 2 RAM.

(c) Calculate the memory stall cycles if number of misses are 10 and miss penalty is 0.3. [7 + 5 + 3]

10. (a) What is Interrupt?

(b) What are the available interrupts in Intel 8085A? Explain each of them.

(c) Draw the Timing diagram of MOV B. [3 + 8 + 4]

11. (a) Draw the Pin diagram of Intel 8085A.

(b) Explain the functionalities of Address, Data and DMA controlling pins.

(c) Explain any five instructions from Arithmetic group of Intel 8085A. [7 + 3 + 5]