

BRAINWARE UNIVERSITY

ODD Semester Examinations 2021-22

Programme – Bachelor of Technology in Computer Science & Engineering - 2019 [B.Tech.(CSE)]

Course Name – Digital Electronics

Course Code – ESC(CSE)302

(Semester III)

	(Semester III)	
Time allotted: 1 Hour 15 Minutes		Full Marks: 60
(Multiple cho	ise type question)	60 x 1 = 60
Choose the correct alternative from the following		
(I) For arithmetic operations which one is faster?		
A) 1's complement	B) 2's complement	
C) 10's complement	D) 9's complement	
(II) If minuend = 0, subtrahend = 1 and borrow input = 0 in a ful	subtractor then the difference output will be	
A) 1	B) 0	
C) Floating	D) High Impedance	
(III) The output of a subtractor is given by (if A, B and X are the i	inputs)	
A) A AND B XOR X	B) A XOR B XOR X	
C) A OR B NOR X	D) A NOR B XOR X	
(IV) In 1:4 demultiplexer, if $S_0 = 1 \& S_1 = 1$, then the output will be		
A) Y ₀	B) Y ₁	
C) Y ₂	D) Y ₃	
(V) Karnaugh map is used:		
A) To draw the digital circuit layout	B) To simplify logical function	
C) To locate different gates in a digital circuit	D) None of these	
(VI) In which operation, carry is obtained?		
A) Subtraction	B) Addition	
C) Multiplication	D) Addition and Subtraction	
(VII) A digital system consists of types of circuits.		
A) 2	В) 3	
C) 4	D) 5	
(VIII) The role of the is to convert the collector current	into a voltage in RTL.	
A) Collector resistor	B) Base resistor	
C) Capacitor	D) Inductor	
(IX) Exclusive-OR (XOR) logic gates can be constructed from wh	at other logic gates?	
A) OR gates only	B) AND gates and NOT gates	
C) AND gates, OR gates, and NOT gates	D) OR gates and NOT gates	
(X) The gates required to build a half adder are		
A) EX-OR gate and NOR gate	B) EX-OR gate and OR gate	
C) EX-OR gate and AND gate	D) EX-NOR gate and AND gate	
(XI) The value of base x is: $(211)_x = (152)_8$		
A) 7	B) 8	
C) 6	D) 5	
(XII) The odd parity output of decimal number 9 is		

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A) 0	B) 1
C) 11	D) 1001
(XIII) Full subtractor is used to perform subtraction of	
A) 4 bits	B) 3 bits
C) 2 bits	D) 8 bits
(XIV) A 4-bit shift register that receives 4 bits of parallel data will shift	
A) Right, one	B) Right, two
C) Left, one	D) Left, three
(XV) Which is an incorrect rule of binary subtraction from the following	207
A) 0 - 0 = 0	B) 0 - 1 = -1
C) $1 - 0 = 1$	D) 0 – 1 = 1 with borrow '1'
(XVI) The NOR gate output will be high if the two inputs are	
A) 0 0	B) 0 1
C) 1 0	D) 1 1
G/ = 0	2)
(XVII) To add two m-bit numbers, the required number of half adders	sis
A) 2m – 1	B) m – 1
C) 2m + 1	D) 2m
(XVIII) Which of the following flip-flop is used as a latch?	
A) J-K flip-flop	B) R-S flip-flop
C) T flip-flop	D) D flip-flop
(XIX) The expression Y=(A+B)(B+C)(C+A) shows the operat	ion
A) AND	B) POS
C) SOP	D) NAND
(XX) In a combinational circuit, the output at any time depends only	on the at that time.
A) Voltage	B) Intermediate values
C) Input values	D) Clock pulses
•	, ·
(XXI) In witch of the following base systems is 123 not a valid number	?
A) Base16	B) Base3
C) Base10	D) Base8
(VVII) Which I are in the feature of all the I are feature?	
(XXII) Which logic is the fastest of all the logic families?	D) 501
A) TTL	B) ECL
C) HTL	D) DTL
(XXIII) The selector inputs to an arithmetic/logic unit (ALU) determine	e the
A) Selection of the IC	B) Arithmetic or logic function
C) Data word selection	D) Clock frequency to be used
C) Data word selection	b) clock frequency to be used
(XXIV) When an input signal A=11001 is applied to a NOT gate serially	, its output signal is
A) 111	B) 00110
C) 10101	D) 11001
(XXV) Divide the binary numbers: 111101 ÷ 1001 and find the remaine	der
A) 10	B) 1010
C) 1100	D) 0011
(VVVII) All logic operations can be obtained by many of	
(XXVI) All logic operations can be obtained by means of	D) OD and NOD anarotic
A) AND and NAND operations	B) OR and NOR operations
C) OR and NOT operations	D) NAND and NOR operations
(XXVII) How many NAND circuits are contained in a 7400 NAND IC?	
A) 1	B) 2
C) 4	D) 8
G) T	<i>2</i> 10
(XXVIII) Convert (0.345) ₁₀ into an octal number:	

A) (0.16050) ₈	B) (0.26050) ₈
C) (0.19450) ₈	D) (0.24040) ₈
(XXIX) The number 140 in octal is equivalent to?	
A) (90) ₁₀	B) (88) ₁₀
C) (86) ₁₀	D) (96) ₁₀
(XXX) Don't care conditions can be used for simplifying Boole	
A) Registers	B) Terms
C) K-maps	D) Latches
(XXXI) If the number of n selected input lines is equal to 2 ^m th	on it requires a select lines
	•
A) 2	B) m
C) n	D) 2n
(XXXII) The excess-3 code for 597 is given by	
A) 100011001010	B) 100010100111
C) 10110010111	D) 10110101101
(XXXIII) The inverter can be produced with how many NAND g	gates?
A) 1	В) 3
C) 2	D) 4
C _j Z	
(XXXIV) In an ECL the output is taken from	
A) Emitter	B) Base
C) Collector	D) Junction of emitter and base
,	•
(XXXV) In the toggle mode a JK flip-flop has-	
A) $J = 0$, $K = 0$	B) J = 1, K = 1
C) $J = 0$, $K = 1$	D) $J = 1, K = 0$
(XXXVI) TTL circuits with "totem-pole" output stage minimize	
A) The power dissipation in RTL	B) The time consumption in RTL
A) The power dissipation in RTLC) The speed of transferring rate in RTL	B) The time consumption in RTLD) Propagation delay in RTL
C) The speed of transferring rate in RTL	D) Propagation delay in RTL
C) The speed of transferring rate in RTL (XXXVII) The excess 3 code of decimal number 26 is	D) Propagation delay in RTL
C) The speed of transferring rate in RTL (XXXVII) The excess 3 code of decimal number 26 is A) 0100 1001	D) Propagation delay in RTL B) 1011001
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(XLIV) In a multiplexer the output depends on its	·
A) Data inputs	B) Select inputs
C) Select outputs	D) None of these
(XLV) Ripple counters are also called	
A) SSI counters	B) Asynchronous counters
C) Synchronous counters	D) VLSI counters
(XLVI) The full form of TCTL is	
A) Transistor-coupled transistor logic	B) Transistor-capacitor transistor logic
C) Transistor-complemented transistor logic	D) Transistor-complementary transistor logic
(XLVII) Which of the following describes the operation of a positive	edge-triggered D flip-flop?
A) If both inputs are HIGH, the output will toggle	B) The output will follow the input on the leading edge of the clock
C) When both inputs are LOW, an invalid state exists	D) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock
(XLVIII) Which of the following is the Universal Flip-flop?	
A) S-R flip-flop	B) J-K flip-flop
C) Master slave flip-flop	D) D Flip-flop
(XLIX) Which of the following circuits come under the class of seque 5. Counter	ential logic circuits? 1. Full adder 2. Full subtractor 3. Half adder 4. J-K flip
A) 1 and 2	B) 2 and 3
C) 3 and 4	D) 4 and 5
(L) The full subtractor can be implemented using	
A) Two XOR and an OR gates	B) Two half subtractors and an OR gate
C) Two multiplexers and an AND gate	D) Two comparators and an AND gate
(LI) Convert the hexadecimal number (1E2) ₁₆ to decimal:	
A) 480	B) 498
C) 482	D) 484
(LII) How many AND gates are required for a 8-to-1 multiplexer?	
A) 5	B) 7
C) 8	D) 6
(LIII) What does minuend and subtrahend denotes in a subtractor?	
A) Their corresponding bits of input	B) Its outputs
C) Its inputs	D) Borrow bits
(LIV) What is one disadvantage of an S-R flip-flop?	
A) It has no Enable input	B) It has a RACE condition
C) It has no clock input	D) Invalid State
(LV) To increase fan-out of the gate in DTL	
A) An additional capacitor may be used	B) An additional transistor and diode may be used
C) An additional resister may be used	D) Only an additional diode may be used
(LVI) TTL is called transistor-transistor logic because both the logic	gating function and the amplifying function are performed by
A) Resistors	B) Bipolar junction transistors
C) One transistor	D) Resistors and transistors respectively
(LVII) How many stages a DTL consist of?	
A) 2	B) 3
C) 4	D) 5
(LVIII) A combinational circuit is one in which the output depends o	on the
A) Input combination at the time	B) Input combination and the previous output
C) Input combination at that time and the previous input combination	D) Present output and the previous output

(LIX) In which operation carry is obtained?	
A) Subtraction	B) Addition
C) Multiplication	D) Both addition and subtraction
(LX) If A, B and C are the inputs of a full adder then	the carry is given by
A) A AND B OR (A OR B) AND C	B) A OR B OR (A AND B) C
C) (A AND B) OR (A AND B)C	D) A XOR B XOR (A XOR B) AND C