BRAINWARE UNIVERSITY

ODD Semester Examinations 2021- 22

Programme – Bachelor of Technology in Computer Science & Engineering - 2020 [B.Tech.(CSE)]

Course Name – Digital Electronics

Course Code – ESC(CSE)302

(Semester III)

Time allotted : 1 Hour 15 Minutes | Full Marks : 60

(Multiple choise type question) | 60 x 1 = 60

Choose the correct alternative from the following

(I) The first step of analysis procedure of SR latch is to _____

A) label inputs B) label outputs

C) label states D) label tables

(II) In a combinational circuit, the output at any time depends only on the _____ at that time.

A) Voltage B) Intermediate values

C) Input values D) Clock pulses

(III) How many stages a DTL consist of?

A) 2 B) 3

C) 4 D) 5

(IV) The excess 3 code of decimal number 26 is_____.

A) 0100 1001 B) 1011001

C) 1000 1001 D) 1001101

(V) The canonical sum of product form of the function y(A,B) = A + B is

A) AB + BB + A'A B) AB + AB' + A'B

C) BA + BA' + A'B' D) AB' + A'B + A'B'

(VI) (A + B)(A' * B') = ?

A) 1 B) 0

C) AB D) AB'

(VII) Standard TTL circuits operate with a __ volt power supply

A) 2 B) 5

C) 4 D) 6

(VIII) The number 140 in octal is equivalent to?

A) $(90)_{10}$ B) $(88)_{10}$

C) $(86)_{10}$ D) $(96)_{10}$

(IX) The binary number 10101 is equivalent to decimal number_____.

A) 19 B) 12

C) 21 D) 27

(X) Which is an incorrect rule of binary subtraction from the following?

A) 0 – 0 = 0 B) 0 – 1 = -1

C) 1 – 0 = 1 D) 0 – 1 = 1 with borrow '1'

(XI) To add two m-bit numbers, the required number of half adders is

A) 2m – 1 B) m – 1

C) 2m + 1 D) 2m

(XII) In which operation carry is obtained?

A) Subtraction
B) Addition
C) Multiplication
D) Both addition and subtraction

(XIII) Let the input of a subtractor is A and B then what the output will be if A = B?

A) 0
B) 1
C) A
D) B

(XIV) To increase fan-out of the gate in DTL

A) An additional capacitor may be used
B) An additional transistor and diode may be used
C) An additional resister may be used
D) Only an additional diode may be used

(XV) Karnaugh map is used:

A) To draw the digital circuit layout
B) To simplify logical function
C) To locate different gates in a digital circuit
D) None of these

(XVI) Full subtractor is used to perform subtraction of _____.

A) 4 bits
B) 3 bits
C) 2 bits
D) 8 bits

(XVII) In a comparator, if we get input as A>B then the output will be _____.

A) 1
B) 0
C) A
D) B

(XVIII) Which logic is the fastest of all the logic families?

A) TTL
B) ECL
C) HTL
D) DTL

(XIX) A combinational circuit is one in which the output depends on the

A) Input combination at the time
B) Input combination and the previous output
C) Input combination at that time and the previous input combination
D) Present output and the previous output

(XX) Convert the hexadecimal number $(1E2)_{16}$ to decimal:

A) 480
B) 498
C) 482
D) 484

(XXI) How many NOT gates are required for the construction of a 4-to-1 multiplexer?

A) 3
B) 4
C) 2
D) 5

(XXII) The inverter can be produced with how many NAND gates?

A) 1
B) 3
C) 2
D) 4

(XXIII) The role of the _____ is to convert the collector current into a voltage in RTL.

A) Collector resistor
B) Base resistor
C) Capacitor
D) Inductor

(XXIV) The full subtractor can be implemented using _____.

A) Two XOR and an OR gates
B) Two half subtractors and an OR gate
C) Two multiplexers and an AND gate
D) Two comparators and an AND gate

(XXV) The odd parity output of decimal number 9 is

A) 0
B) 1
C) 11
D) 1001

(XXVI) All logic operations can be obtained by means of _____.

A) AND and NAND operations
B) OR and NOR operations
C) OR and NOT operations
D) NAND and NOR operations

(XXVII) ECL's major disadvantage is that

A) It requires more power
B) It's fan-out capability is high
C) It creates more noise
D) It is slow

(XXVIII) The full form of TCTL is _____.

A) Transistor-coupled transistor logic
B) Transistor-capacitor transistor logic
C) Transistor-complemented transistor logic
D) Transistor-complementary transistor logic

(XXIX) One multiplexer can take the place of _____

A) Several SSI logic gates
B) Combinational logic circuits
C) Several Ex-NOR gates
D) Several SSI logic gates or combinational logic circuits

(XXX) In a multiplexer the output depends on its _____.

A) Data inputs
B) Select inputs
C) Select outputs
D) None of these

(XXXI) The expression Y=(A+B)(B+C)(C+A) shows the _____ operation.

A) AND
B) POS
C) SOP
D) NAND

(XXXII) If the number of n selected input lines is equal to 2^m then it requires _____ select lines.

A) 2
B) m
C) n
D) 2n

(XXXIII) Don't care conditions can be used for simplifying Boolean expressions in _____.

A) Registers
B) Terms
C) K-maps
D) Latches

(XXXIV) When an input signal A=11001 is applied to a NOT gate serially, its output signal is

A) 111
B) 00110
C) 10101
D) 11001

(XXXV) If A and B are the inputs of a half adder, the sum is given by

A) A AND B
B) A OR B
C) A XOR B
D) A EX-NOR B

(XXXVI) Divide the binary numbers: 111101 ÷ 1001 and find the remainder

A) 10
B) 1010
C) 1100
D) 0011

(XXXVII) In the toggle mode a JK flip-flop has-

A) J = 0, K = 0
B) J = 1, K = 1
C) J = 0, K = 1
D) J = 1, K = 0

(XXXVIII) The full form of ECL is _____.

A) Emitter-collector logic
B) Emitter-complementary logic
C) Emitter-coupled logic
D) Emitter-cored logic

(XXXIX) On subtracting $(001100)_2$ from $(101001)_2$ using 2's complement, we get _____.

A) 1101100
B) 011101
C) 11010101
D) 11010111

(XL) The excess-3 code for 597 is given by _____.

A) 100011001010
B) 100010100111
C) 10110010111
D) 10110101101

(XLI) Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?

A) OR gates only
B) AND gates and NOT gates
C) AND gates, OR gates, and NOT gates
D) OR gates and NOT gates

(XLII) Which of the following flip-flop is used as a latch?

A) J-K flip-flop
B) R-S flip-flop
C) T flip-flop
D) D flip-flop

(XLIII) Which of the following circuits come under the class of sequential logic circuits? 1. Full adder 2. Full subtractor 3. Half adder 4. J-K flip 5. Counter

A) 1 and 2
B) 2 and 3
C) 3 and 4
D) 4 and 5

(XLIV) When two 16-input multiplexers drive a 2-input MUX, what is the result?

A) 2-input MUX
B) 4-input MUX
C) 16-input MUX
D) 32-input MUX

(XLV) For arithmetic operations which one is faster?

A) 1's complement
B) 2's complement
C) 10's complement
D) 9's complement

(XLVI) In 1:4 demultiplexer, if $S_0 = 1$ & $S_1 = 1$, then the output will be _____.

A) Y_0
B) Y_1
C) Y_2
D) Y_3

(XLVII) What does minuend and subtrahend denotes in a subtractor?

A) Their corresponding bits of input
B) Its outputs
C) Its inputs
D) Borrow bits

(XLVIII) The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____.

A) Combinational circuits
B) Sequential circuits
C) Latches
D) Flip-flops

(XLIX) A digital multiplexer is a combinational circuit that selects

A) One digital information from several sources and transmits the selected one
B) Many digital information and convert them into one
C) Many decimal inputs and transmits the selected information
D) Many decimal outputs and accepts the selected information

(L) The NOR gate output will be high if the two inputs are _____.

A) 0 0
B) 0 1
C) 1 0
D) 1 1

(LI) $(734)_8 = (?)_{16}$

A) C1D
B) DC1
C) 1CD
D) 1DC

(LII) The largest two digit hexadecimal number is _____.

A) $(FE)_{16}$
B) $(FD)_{16}$
C) $(FF)_{16}$
D) $(EF)_{16}$

(LIII) The value of base x is: $(211)_x = (152)_8$

A) 7
B) 8
C) 6
D) 5

(LIV) Which of the following is the Universal Flip-flop?

A) S-R flip-flop
B) J-K flip-flop
C) Master slave flip-flop
D) D Flip-flop

(LV) If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____

A) SET
B) RESET
C) Clear
D) Invalid

(LVI) Which of the following describes the operation of a positive edge-triggered D flip-flop?

A) If both inputs are HIGH, the output will toggle
B) The output will follow the input on the leading edge of the clock
C) When both inputs are LOW, an invalid state exists
D) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock

(LVII) TTL circuits with "totem-pole" output stage minimize

A) The power dissipation in RTL
B) The time consumption in RTL
C) The speed of transferring rate in RTL
D) Propagation delay in RTL

(LVIII) What is one disadvantage of an S-R flip-flop?

A) It has no Enable input
B) It has a RACE condition
C) It has no clock input
D) Invalid State

(LIX) The output of a subtractor is given by (if A, B and X are the inputs)_____

A) A AND B XOR X

B) A XOR B XOR X

C) A OR B NOR X

D) A NOR B XOR X

(LX) In which operation, carry is obtained?

A) Subtraction

B) Addition

C) Multiplication

D) Addition and Subtraction