BRAINWARE UNIVERSITY

ODD Semester Examinations 2021- 22

Programme – Bachelor of Technology in Electronics & Communication Engineering - 2019 [B.Tech.(ECE)]

Course Name – Digital System Design

Course Code – PCC-EC302

(Semester III)

Time allotted : 1 Hour 15 Minutes | Full Marks : 60

(Multiple choise type question) | 60 x 1 = 60

Choose the correct alternative from the following

(I) Which of the following combinations of logic gates can decode binary 1101?

A) One 4-input AND gate
B) One 4-input AND gate, one inverter
C) One 4-input AND gate, one OR gate
D) One 4-input NAND gate, one inverter

(II) The transparent latch is

A) an SR latch
B) a D latch
C) a T latch
D) a J-K latch

(III) The following switching functions are to be implemented using a decoder: f1 = ∑m (1, 2, 4, 8, 10, 14), f2 = ∑m (2, 5, 9, 11), f3 = ∑m (2, 4, 5, 6, 7) The minimum configuration of decoder will be _____

A) 2 to 4 line
B) 3 to 8 line
C) 4 to 16 line
D) 5 to 32 line

(IV) The functional difference between an S-R flip-flop and J-K flip-flop is that

A) J-K flip-flop is faster than S-R flip-flop
B) J-K flip-flop has a feedback path
C) J-K flip-flop accepts both inputs 1
D) J-K flip-flop does not require external clock

(V) When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero

A) Sign-magnitude
B) 1's complement
C) 2's complement
D) 9's complement

(VI) The NOR gate output will be high if the two inputs are

A) 0
B) 1
C) 10
D) 11

(VII) A flip-flop can store

A) one bit of data
B) two bits of data
C) three bits of data
D) any number of bits of data

(VIII) Which of following cannot be accessed randomly

A) DRAM
B) SRAM
C) ROM
D) Magnetic tape

(IX) The output of a JK flipflop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the following conditions

A) By applying J = 0, K = 0 and using a clock
B) By applying J = 1, K = 0 and using the clock
C) By applying J = 1, K = 1 and using the clock
D) By applying a synchronous preset input

(X) The minimum number of flip-flops required for a mod-12 ripple counter is

A) 3
B) 4
C) 6
D) 12

(XI) A device which converts BCD to Seven Segment is called

A) Encoder B) Decoder
C) Multiplexer D) Demultiplexer

(XII) The decimal equivalent of Binary number 10101 is
A) 21 B) 31
C) 26 D) 28

(XIII) The MSI chip 7474 is
A) Dual edge triggered JK flip-flop (TTL) B) Dual edge triggered D flip-flop (CMOS)
C) Dual edge triggered D flip-flop (TTL) D) Dual edge triggered JK flip-flop (CMOS)

(XIV) When an inventer is placed between the inputs of an S-R flip-flop, the resulting flip-flop is a
A) J-K flip-flop B) master-slave flip-flop
C) T flip-flop D) D flip-flop

(XV) For JK flipflop J = 0, K=1, the output after clock pulse will be
A) 1 B) no change
C) 0 D) high impedance

(XVI) ASCII and EBCDIC codes are
A) BCD codes B) numeric codes
C) alphanumeric codes D) error correcting codes

(XVII) Which IC is used for the implementation of 1-to-16 DEMUX?
A) IC 74154 B) IC 74155
C) IC 74139 D) IC 74138

(XVIII) Which of the following logic circuits accept two binary digital on inputs and produces two binary digital , a sum bit and carry bit on its outputs?
A) full adder B) half-adder
C) serial adder D) parallel adder

(XIX) A full-adder can be realized using
A) one half-adder, two OR gates B) two half-adder, one OR gates
C) two half-adders, two OR gates D) two half-adders, one AND gates

(XX) The primary advantage of RTL technology was that
A) It results as low power dissipation B) It uses a minimum number of resistors
C) It uses a minimum number of transistors D) It operates swiftly

(XXI) The 2's complement of the number 1101101 is
A) 101110 B) 111110
C) 110010 D) 0010011

(XXII) The hexadecimal number 'A0' has the decimal value equivalent to
A) 80 B) 256
C) 100 D) 160

(XXIII) The Boolean expression $\bar{A}\bar{B}C+\bar{A}BC+A\bar{B}C+ABC$ is equal to
A) A B) B
C) C D) None of these

(XXIV) The commercially available 8-input multiplexer integrated circuit in the TTL family is
A) 7495 B) 74153
C) 74154 D) 74151

(XXV) PAL and PLA are known as
A) CPLD B) SPLD
C) FPLD D) GPLD

(XXVI) Minimum number of two input NAND gates required to realize XNOR gate is
A) 3 B) 4
C) 5 D) 6

(XXVII) How many select lines will a 32:1 multiplexer will have

A) 5 B) 8

C) 9 D) 11

(XXVIII) For a flip-flop with provisions of preset and clear

A) preset and clear operations are performed simultaneously B) while presetting , clear is disabled

C) while clearing , clear is disabled D) Both while presetting , clear is disabled and while clearing , clear is disabled

(XXIX) A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be

A) 15 ns B) 30 ns

C) 45 ns D) 60 ns

(XXX) The access time of ROM using bipolar transistors is about

A) 1 sec B) 1 msec

C) 1 µsec D) 1 nsec.

(XXXI) Knowledge of binary number system is required for designers of computers and other digital systems because

A) it is easy to learn binary number system B) it is easy to learn Boolean algebra

C) it is easy to use binary codes D) the devices used in these systems operate in binary

(XXXII) EDA tools are for

A) Circuit designers B) Device engineers

C) Chip designers D) Fabrication designers

(XXXIII) ECL's major disadvantage is that -

A) It requires more power B) It's fan-out capability is high

C) It creates more noise D) It is slow

(XXXIV) K-Map follows

A) binary code B) ASCII code

C) BCD code D) gray code

(XXXV) When the set of input data to an even parity generator is 0111, the output will be

A) 1 B) 0

C) Unpredictable D) Depends on the previous input

(XXXVI) In VHDL sequential statements are defined in

A) architecture B) process

C) package D) none of these

(XXXVII) Which of following consume minimum power

A) TTL B) CMOS

C) DTL D) RTL

(XXXVIII) A multiplexer is also known as a data

A) accumulator B) restorer

C) selector D) distributor

(XXXIX) High level synthesis is also known as

A) behavioral synthesis B) structural synthesis

C) architectural level synthesis D) all of these

(XL) Convert binary number into gray code: 100101

A) 101101 B) 001110

C) 110111 D) 111001

(XLI) The number of select lines for a 8 – to – 1 multiplexer is_____.

A) 2 B) 3

C) 4 D) 5

(XLII) The decimal equivalent of $(1100)_2$ is

A) 12 B) 16
C) 18 D) 20

(XLIII) The number of control lines for 32 to 1 multiplexer is
A) 4 B) 5
C) 16 D) 6

(XLIV) Shifting a register content to left by one bit position is equivalent to
A) division by two B) addition by two
C) multiplication by two D) subtraction by two

(XLV) $(734)_8 = (\ )_{16}$
A) C 1 D B) D C 1
C) 1 C D D) 1 D C

(XLVI) 1's complement representation of decimal number of -17 by using 8 bit representation is
A) 1110 1110 B) 1101 1101
C) 1100 1100 D) 0001 0001

(XLVII) Data can be changed from special code to temporal code by using
A) shift registers B) counters
C) combinational circuits D) A/D converters

(XLVIII) The logic 0 level of a CMOS logic device is approximately
A) 1.2 volts B) 0.4 volts
C) 5 volts D) 0 volts

(XLIX) What is the binary equivalent of the decimal number 368 _____.
A) 101110000 B) 110110000
C) 111010000 D) 111100000

(L) The number of flip flops contained in IC 7490 is
A) 2 B) 3
C) 4 D) 1

(LI) BCD subtractions is performed by using
A) 1's complement representation B) 2's complement representation
C) 5's complement representation D) 9's complement representation

(LII) How many Flip-Flops are required for mod–16 counter?
A) 5 B) 6
C) 3 D) 4

(LIII) The digital logic family which has the lowest propagation delay time is
A) ECL B) TTL
C) CMOS D) PMOS

(LIV) Parallel adders are
A) combinational logic circuits B) sequential logic circuits
C) Both combinational logic circuits and sequential logic circuits D) None of these

(LV) A demultiplexer is a
A) 1-to-N device B) N-to-1 device
C) 1-to-1 device D) N-to-N device

(LVI) How many two input AND gates are required to realize Y = CD+EF+G
A) 4 B) 5
C) 3 D) 2

(LVII) Which of the following is the fastest logic?
A) ECL B) TTL
C) CMOS D) LSI

(LVIII) Binary subtraction of 100101 – 011110 is

A) 000111 B) 111000

C) 10101 D) 101010

(LIX) A disadvantage of DTL is

A) The input transistor to the resister B) The input resister to the transistor

C) The increased fan-in D) The increased fan-out

(LX) The way to speed up DTL is to add an across intermediate resister is

A) Small “speed-up” capacitor B) Small “speed-up” transistor

C) Large “speed-up” capacitor D) Large ” speed-up” transistor