BRAINWARE UNIVERSITY

Course – MCA

Digital Electronics (MCA 101)

(Semester – 1)

Time allotted: 3 Hours **Full Marks : 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Questions) 1 x 10 = 10

1. Choose the correct alternative for the following : (*Any Ten*)

(i) The SOP form of logical expression is most suitable for designing logic circuits using only

a) XOR gates b) NOR gates

c) NAND gates d) OR gates

(ii) The r's complement of number N_r is

a) r - 1's complement + 1 b) r^m - N

c) both (a) & (b) d) none of these

(iii) Floating point representation is the combination of

a) integer and fraction b) mantissa and exponent

c) long integer and double d) integer and double

(iv) When race condition occur in SR flip-flop?

a) S = 0, R = 0 b) S = 1, R = 0

c) S = 0, R = 1 d) S = 1, R = 1

(v) The gray code of decimal 7 is

a) 0111 b) 1011

c) 0100 d) 0101

(vi) A demultiplexer has

a) one data input and a number of selection inputs, and they have several outputs

b) one input and one output

c) several inputs and several outputs

d) several inputs and one output.

(vii) A latch is _____ sensitive.

a) both level and edge b) edge

c) level d) none of these

(viii) How many bits are required to store one BCD digit ?

a) 1 b) 2

c) 3 d) 4

(ix) In binary number system the first digit (bit) from right to left is called as

a) LSB b) MSB

c) First Bit d) Last Bit

(x) In an SR latch built from NOR gates, which condition is not allowed

a) S=0, R=0 b) S=0, R=1

c) S=1, R=0 d) S=1, R=1

(xi) A Binary number system has how many digits?

a) 0 b) 1

c) 2 d) 10

(xii) A Nibble is equal to _____ bit(s)

a) 0 b) 4

c) 2 d) 10

Group – B

(Short Answer Type Question) 3 x 5 = 15

Answer any *three* from the following:

2. What is truth table? Why is it called so?

3. Why NAND gate is called universal logic gate?

4.

(a) Simplify using K-map : A'B'C + A'BC + AB'C +ABC

(b) Write some disadvantages of K-map. 3 + 2 = 5

5. Draw the Block Diagram, Boolean Expression, Logic Symbol, IEEE Symbol and Truth Table of XOR Gate.

6. Design a 16 X 1 MUX using 4 X 1 MUX only.

Group – C

(Long Answer Type Question) 3 x 15 = 45

Answer any *three* from the following:

7.

(a) X and Y are two successive numbers in a number system. If XY = 33 and YX = 39, find the value of the X and Y.

(b) Convert the following into Binary, Octal and Hexadecimal (Assuming the value in Base 10) -

$$7\frac{23}{47}$$

(c) Find the value of x for the following equation - $(100)_X = (22)_7$ (5 + 5 + 5)

8.

(a) Using K-map method minimize the following expression:

$F(w, x, y, z) = \Sigma (1, 5, 6, 9, 12, 13, 14) + d \Sigma (2, 4)$

(b) Implement XOR gate using NAND gate.

(c) Implement NOR gate using NAND gate. (5 + 5 + 5)

9.

(a) Design a Full Adder using Basic Gates only.

(b) Design a 8 X 3 Encoder using Basic Gates only.

(c) Why Multiplexer is called Data Selector? (7 + 5 + 3)

10.

(a) What do you mean by the term Latch? Explain.

(b) Design a S-R Flip-Flop using NAND Gates only.

(c) Differentiate between Latch and Flip-Flop. (3 + 6 + 6)

11.

(a) Design a Mod 8 Counter using J-K Flip-Flop.

(b) What is the difference between Synchronous and Asynchronous Counter?

(c) Design a SIPO Register using S-R Flip-Flop. (7 + 3 + 5)