BRAINWARE UNIVERSITY

Course –MCA

Digital Electronics (MCA101)

(Semester – 1)

Time allotted: 3 Hours **Full Marks: 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Question) 10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) How many address bits are needed to select all memory locations in the 2118, 16K × 1 RAM?

a. 8. b. 14.

c. 10. d. 16.

(ii) Propagation delay time, t_{PLH}, is measured from the _____.

a. Triggering edge of the clock pulse to the LOW-to-HIGH transition of the output.

b. Triggering edge of the clock pulse to the HIGH-to-LOW transition of the output.

c. Preset input to the LOW-to-HIGH transition of the output.

d. Clear input to the HIGH-to-LOW transition of the output.

(iii) Minimum no. of NAND gates required to design a Full Subtractor

a. 2. b. 2.

c. 15. d. 9.

(iv) On a master-slave flip-flop, when is the master enabled?

a. When the gate voltage is low b. When the gate voltage is high

c. Both of the above d. None of the these

(v) To make a T flip-flop using JK flip-flop it requires?

a. J and sorted with clock pulse.

b. J and K both are sorted with a NOT gate.

c. J and K are sorted with XOR gate.

d. J and K are directly sorted.

(vi) Which statement BEST describes the operation of a negative-edge-triggered D flip-flop?

a. The logic level at the D input is transferred to Q on NGT of CLK.
b. The Q output is ALWAYS identical to the CLK input if the D input is HIGH.
c. The Q output is ALWAYS identical to the D input when CLK = PGT.
d. The Q output is ALWAYS identical to the D input.

(vii) Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:

a. Input clock pulses are applied only to the first and last stages.
b. Input clock pulses are applied only to the last stage.
c. Input clock pulses are not used to activate any of the counter stages.
d. Input clock pulses are applied simultaneously to each stage.

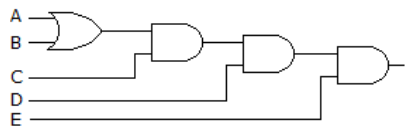
(viii) How many flip-flops are required to make a MOD-32 binary counter?

a. 3.
b. 45.
c. 6.
d. 5.

(ix) A MOD-16 ripple counter is holding the count 10012. What will be the count after 31 clock pulses?

a. 1000_2.
b. 1010_2.
c. 1011_2.
d. 1101_2.

(x)



a. $[[C(A+B)D]E^{/}]$
b. $[C(A+B)D+E^{/}]$
c. C(A+B)DE.
d. ABCDE

Group – B

(Short Answer Type Question) 3 x 5 = 15

Answer any *three* from the following

2. (a) Differentiate latch and flip-flop. [2]
   (b) What is digital pulse? [1]
   (c) Draw a diagram and specify rise time, fall time and duration (width) of the pulse. [1]
   (d) What is NGT and PGT? [1]
3. Draw a 2's complement circuit and test with an example. [5]

4. (a) What is the function of a D flip-flop that triggers only on positive-going transitions? [3]
   (b) Illustrate this by drawing the waveforms. [2]
5. How can we perform parallel data transfer by using D flip-flop? [5]
6. (a) Draw the truth table for 3-bit message which generate odd parity bit. [2]
   (b) Draw the circuit for odd parity generator and checker. [3]

Group – C

(Long Answer Type Question) 3 x 15 = 45

Answer any *three* from the following

7. (a) Draw the truth table and circuit for 1 to 8 Demultiplexer. [5]
   (b) The logic expression of the output of a four input digital circuit is given below.
   $B_3 = \sum_m (8, 9, 10, 11, 12, 13, 14, 15)$
   $B_2 = \sum_m (4, 5, 6, 7, 8, 9, 10, 11)$
   $B_1 = \sum_m (2, 3, 4, 5, 8, 9, 14, 15)$
   $B_0 = \sum_m (1, 2, 4, 7, 8, 11, 13, 14)$
   Simplify the above expressions by using K map and draw the logic circuit using XOR gate only. [10]

8. (a) Draw the diagram for BCD to 7 segment decoder driving a common anode 7 segment LED display (Both the VCC of driver and display are 5V). [3]
   (b) Each segment of a typical 7 segment LED display is rated to operate at 12mA and 2.5V for normal brightness. Calculate the value of current limiting resistor needed to produce approximately 12mA per segment (Both the VCC of driver and display are 5V). [2]
   (c) $a = \sum_m (0, 2, 3, 5, 6, 7, 8, 9) + \sum_d (10, 11, 12, 13, 14, 15)$
   $b = \sum_m (0, 1, 2, 3, 4, 7, 8, 9) + \sum_d (10, 11, 12, 13, 14, 15)$
   $c = \sum_m (0, 1, 3, 4, 5, 6, 7, 8, 9) + \sum_d (10, 11, 12, 13, 14, 15)$
   $d = \sum_m (0, 2, 3, 5, 6, 8, 9) + \sum_d (10, 11, 12, 13, 14, 15)$
   $e = \sum_m (0, 2, 6, 8) + \sum_d (10, 11, 12, 13, 14, 15)$
   $f = \sum_m (0, 4, 5, 6, 8, 9) + \sum_d (10, 11, 12, 13, 14, 15)$
   $g = \sum_m (2, 3, 4, 5, 6, 8, 9) + \sum_d (10, 11, 12, 13, 14, 15)$
   Draw circuit by simplifying the K map for each output [7+3]

9. (a) Draw the circuit diagram of a clocked J-K flip-flop using only two input NAND gates. [5]
   (b) Implement $Y = (AB)' + A + (B+C)'$ only using NAND gates. [5]
   (c) Realize $Y = (A+C)(A+D')(A+B+C')$ using NOR gates. [5]

10.	(a)	Design a 4-bit ripple counter with block diagram.	[2]
	(b)	Draw the wave forms of the outputs depending on the input clock signal and describe the process briefly by drawing the truth table.	[4+2+2]
	(c)	Comment on the frequency division or frequency scaling of the above designed ripple counter.	[3]
	(d)	Why it is called a MOD – 16 ripple counter?	[2]
11.	(a)	Define uni - directional, bi- directional and Universal Shift Register?	[1+1+1]
	(b)	List out the capabilities of shift registers.	[5]
	(c)	Draw the circuit diagram of a 4 – bit universal shift registers.	[7]