



BRAINWARE UNIVERSITY

Course – BCA

Digital Electronics (BCA102/BCAC103)

(Semester – 1)

Time allotted: 3 Hours

Full Marks : 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Questions)

10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) The 9's complement of $(52500)_{10}$ is

a. 47499

b. 46499

c. 58500

d. 58599

(ii) Minimum number of NAND gates required to implement XOR gate is

a. 1

b. 2

c. 3

d. 4

(iii) Signed 1's complement representation of the number $(-13)_{10}$ is

a. 10010

b. 11101

c. 10011

d. 11100

(iv) The octal equivalent of the number $(110010001)_2$ is

a. 631

b. 620

c. 600

d. 621

- (v) The packed format in EBCDIC-8 bit format of the numeric value -345 is
- | | |
|-----------|---------|
| a. F3F4F5 | b. F345 |
| c. D3D4D5 | d. 345D |
- (vi) The hexadecimal coding of the word “BCA” represented in ASCII 7 bit is
- | | |
|-----------|-----------|
| a. 404142 | b. 414243 |
| c. 424344 | d. 424341 |
- (vii) 4 bit Parallel Adder can be implemented using
- | | |
|-----------------------------------|------------------------------------|
| a. 3 Full Adders and 1 Half Adder | b. 2 Full Adders and 2 Half Adders |
| c. 1 Full Adder and 3 Half Adders | d. 4 Half Adders |
- (viii) The 6 bit sign magnitude representation of the decimal number (-18) is
- | | |
|------------|-----------|
| a. 1 01101 | b. 101111 |
| c. 110010 | d. 101010 |
- (ix) Invalid state is observed in SR flip flop if
- | | |
|------------|------------|
| a. S=R=0 | b. S=1 R=0 |
| c. S=0 R=1 | d. S=R=1 |
- (x) Total number of Flip flops required to implement the sequence 4,0,10,2,16,3 is
- | | |
|------|------|
| a. 3 | b. 4 |
| c. 5 | d. 6 |

Group – B

(Short Answer Type Questions)

3 x 5 = 15

Answer any *three* from the following

2. A combinational circuit is defined by the following three functions:
 $F1 = \bar{x}\bar{y} + xy\bar{z}$, $F2 = \bar{x} + y$, $F3 = xy + \bar{x}y$
 Design the circuit with a decoder and external gates. [5]
3. Explain the Race around condition in JK flip flop. [5]
4. Construct an 8X1 Multiplexer implemented using basic gates. Estimate the total cost required to implement 2^n to 1 Multiplexer. [3+2]
5. Explain the working principle of 4 bit SISO shift register. [5]

6. Obtain the simplified expression in sum of product terms for the following Boolean function:
 $F(A,B,C) = \bar{A}B + B\bar{C} + \bar{B}\bar{C}$ [5]

Group – C

(Long Answer Type Questions)

3 x 15 = 45

Answer any *three* from the following

7. (a) Explain the working principle of 1X8 Demultiplexer. [5]
 (b) Design a combinational circuit which accepts a three-bit number and output binary number equal to the square of the input number. [10]
8. (a) Explain the working principle of 3X8 decoder. [5]
 (b) A combinational circuit is defined by the following two functions:
 $F1 = \sum(0,3)$
 $F2 = \sum(0,2,3,7)$
 Implement the combinational circuit using decoder and external gates. [10]
9. (a) Explain the Full Subtractor operation with its circuit diagram. [5]
 (b) Implement the Full Subtractor operation using Multiplexer. [5]
 (c) Design a circuit using Multiplexer and Counter to generate the following sequence:10010100 [5]
10. (a) Design a synchronous Decade counter. [10]
 (b) Design D flip flop using SR flip flop. [5]
11. (a) Explain the working principle of clocked SR flip flop. [5]
 (b) Design a binary counter having the following repeated binary sequence.
 0,1,2,3,4,5,6.
 Use T flip flop. [10]