

**BRAINWARE UNIVERSITY****Course – B.Sc.(CS)****Computer Organisation and Architecture (BCS302)****(Semester – 3)****Time allotted: 3 Hours****Full Marks : 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A**(Multiple Choice Type Questions)****10 x 1 = 10**

1. *Choose the correct alternative from the following*

(i) The decoded instruction is stored in

- | | |
|--------------|--------------|
| a. IR | b. IR |
| c. Registers | d. Registers |

(ii) The fastest data access is provided using

- | | |
|-----------|--------------|
| a. Caches | b. DRAMs |
| c. SRAMs | d. Registers |

(iii) A hard disk with 20 surfaces will have _____ heads.

- | | |
|-------|-------|
| a. 10 | b. 5 |
| c. 1 | d. 20 |

(iv) The binary address issued to data or instructions are called as

- | | |
|------------------------|---------------------|
| a. Physical address | b. Location address |
| c. Relocatable address | d. Logical address |

(v) Convert the binary number (1111000011110000) to hexadecimal number

- | | |
|---------|---------|
| a. 1010 | b. 1010 |
| c. 7070 | d. 7070 |

(vi) 8085 microprocessor operates at a frequency of

- | | |
|----------|------------|
| a. 6 MHz | b. 3.2 MHz |
| c. 5 MHz | d. 3 MHz |

- (vii) The address line required for 16 k byte memory chip are
- | | |
|-------|-------|
| a. 13 | b. 13 |
| c. 15 | d. 15 |
- (viii) Which of the following is a user programmable register?
- | | |
|----------------------------|----------------------------|
| a. Memory Address Register | b. Memory Address Register |
| c. Program Counter | d. Program Counter |
- (ix) RST 7.5 interrupt is
- | | |
|------------------------|----------------------------|
| e. Vectored & Maskable | f. Vectored & Non-Maskable |
| g. Direct & Maskable | h. Direct & Non-Maskable |
- (x) 2's Complement of 10101011 is
- | | |
|-------------|-------------|
| a. 01010101 | b. 01010101 |
| c. 01110101 | d. 01110101 |

Group – B

(Short Answer Type Questions)

3 x 5 = 15

Answer any *three* from the following

- | | |
|---|-----|
| 2. Explain Dynamic RAM. | [5] |
| 3. Describe the Harvard architecture. | [5] |
| 4. Differentiate between Fixed Point and Floating Point Number. | [5] |
| 5. What do you mean by Cache Mapping? Explain. | [5] |
| 6. What are the advantages and disadvantages of Asynchronous BUS? | [5] |

Group – C

(Long Answer Type Questions)

3 x 15 = 45

Answer any *three* from the following

- | | |
|---|------|
| 7. (a) What are the special purpose registers available in Intel 8085A? | [5] |
| (b) Explain each of these special purpose registers. | [10] |
| 8. (a) Describe the general PC BUS architecture. | [5] |
| (b) Find the value of x for the following equation - $(100)_b = (22)_7$ | [5] |
| (c) Convert $(BCD)_{16}$ to BCD Code. | [5] |
| 9. (a) Write the advantages and disadvantages of Pipeline architecture. | [7] |
| (b) What is the utility of Stack Pointer and Program Counter? | [3] |
| (c) Explain Instruction Pipeline. | [5] |
| 10. (a) Explain Input/Output Interrupt Code Registers (IOIC). | [3] |
| (b) Multiply – 5 and 2 using Booth's Multiplication Algorithm. | [8] |
| (c) What is MDRAM and PSRAM? Explain in brief. | [4] |
| 11. (a) What do you mean by Single and Double Precision Format? | [2] |
| (b) Compare the storage layout of Single and Double Precision Floating Point Numbers. | [5] |
| (c) State the conditions for having NaN. | [3] |
| (d) Explain Flag Register with respect to Intel 8085A. | [5] |