

BRAINWARE UNIVERSITY

Course -B.Sc. (HN)

Digital Electronics and Instrumentation (EC301)

(Semester - 3)

Time allotted: 3 Hours Full Marks: 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group -A

(Multiple Choice Type Questions)

 $10 \times 1 = 10$

- 1. Choose the correct alternative from the following (i) Decimal equivalent of an octal number (137.21)₈ is a. $(952.65)_{10}$ b. (95.265)₁₀ c. (9526.5)₁₀ d. (9.5265)₁₀ (ii) Electrostatic type instruments are primarily used as a. ammeters b. watt meters c. voltmeters d. ohm meters (iii) Frequency can be measured by using
 - e. Maxwell's bridge

- f. Schering bridge
- g. Heaviside Campbell bridge
- h. Wien's bridge
- (iv) The source of emission of electrons in a CRT is
 - a. p-n junction diode

- b. barium and strontium oxide coated
 - cathode

c. accelerating anodes

d. post-accelerating anodes

(v)	The NOR gate is OR gate followed by		
	a. AND gate	b. NAND gate	
	c. NOT gate	d. none of the these	
(vi)	Which number system has a base of 16		
	a. Decimal	b. Octal	
	c. Hexadecimal	d. none of these	
(vii)	A flip-flop has		
	a. one stable state	b. two stable states	
	c. no stable state	d. none of these	
(viii)	The Q factor of a coil at the resonant frequency 1.5 MHz of an LCR series circuit is		
	150. The bandwidth is		
	a. 225 MHz	b. 1.06 MHz	
	c. 10 KHz	d. none of these	
(ix)	A full adder circuit has		
	a. two inputs and one output	b. two inputs and two	outputs
	c. two inputs and three outputs	d. three inputs and two	ooutputs
(x)	The bandwidth of a CRO is 20 MHz. The fastest rise time that a sine wave can be		
	accurately reproduced by the instrument is given as		
	a. 35 ns	b. 35 μs	
	c. 17.5 ns	d. 0.17 μs	
	(Short Answer	up – B Type Questions) from the following)	
2.	Write notes on i) Noise mercin	ii) Ean out iii) Ean in iv	$3 \times 5 = 15$
۷.	Write notes on i) Noise margin ii) Fan-out iii) Fan-in iv		
3.	Propagation delay v) Power dissipation Write down the basic features of i)DTL ii) TTL iii) ECL iv) MOS		[1+1+1+1+1]
٥.			
4	logic v) CMOS logic Draw the circuit diagram of a positive logic OP gate with two		[1+1+1+1+1]
4.	Draw the circuit diagram of a positive logic OR gate with two diodes and explain its operation. Give its logic symbol and the truth		
	-	e its logic symbol and the truth	
	table		[3+2]

5. The four impedances of an a.c bridge are $Z_1 = 400 \Omega \angle 50^{\circ}$, $Z_2 = 200 \Omega \angle 40^{\circ}$, $Z_3 = 800 \Omega \angle -50^{\circ} \& Z_4 = 400 \Omega \angle 20^{\circ}$. Find out [5] whether the bridge is balanced under these conditions or not. 6. (a) Show that $\overline{A}(\overline{A}+BC)+\overline{A}(B+C)=\overline{A}$ [3] (b) Find the octal equivalent of $(869.625)_{10}$ [2] Group - C (Long Answer Type Questions) (Answer any *three* from the following) $3 \times 15 = 45$ 7. (a) i) Find the decimal equivalent of (2FF)₁₆. ii) Find the octal equivalent of (879.625)₁₀. iii) Illustrate 1'S complement and 2'S complement. iv) $ABC + A\overline{B}C + AB\overline{C} = A(B+C)$ [2+2+2+2](b) i) State De-Morgan's theorem for more than two variables. ii) Establish the action of NAND gate as Universal gate. [2+5]8. (a) Write short notes on Anderson bridge. [8] (b) What is Q factor relating to series LCR circuit? What is its unit? [1+1](c) A coil of resistance 10Ω is connected in the Q-meter circuit. Resonance [5] occurs at a frequency of 1MHz with the tuning capacitor being set at 65pF. Calculate the % change in the value of Q, if additional resistance of 0.02Ω is used across the oscillator circuit. (a) Describe how a NOT gate is implemented by using BJT. Also, show 9. how the circuit resistances are calculated. [3+3](b) Write down the Boolean expression of output Y of XOR gate. Show how it can be realized by using AND, OR and NOT gates. Present the logic symbol for XOR gate. [1+3+1](c) What is half adder? Give its symbol and truth table. How can it be [1+1+2]implemented with logic gates?

- 10. (a) Write the working principle of CRO with appropriate block diagram. [8]
 - (b) Draw and explain D/A weighted resistor network for 4 bit input. [7]
- 11. (a) Draw circuit diagram to show how an RS flip-flop can be converted [1+4+2] into JK flip-flop. Explain its working principle. Give its truth table.
 - (b) How can you design a 1 to 4 de-multiplexer using basic gates. Give its [4+1+2+1] block diagram. Write down the Boolean expression of output and its truth table.