BRAINWARE UNIVERSITY

Term End Examination 2018 - 19

Programme – Bachelor of Computer Applications / Bachelor of Science (Honours) in Computer Science

Course Name – Computer Organization and Architecture

Course Code – BCSE010603

(Semester – 1)

Time allotted: 3 Hours **Full Marks: 70**

[The figure in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Question) 10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) Which is not a type of ROM?

a. EPROM b. SROM

c. PROM d. EEPROM

(ii) ISP stands for

a. Instruction Set Processor b. Information standard processing

c. Interchange Standard Protocol d. Interrupt service procedure

(iii) The internal Components of the processor are connected by

a. Processor intra-connectivity circuitry b. Processor bus

c. Memory bus d. Rambus

(iv) The number successful accesses to memory stated as a fraction is called as

a. Hit rate b. Miss rate

c. Success rate d. Access rate

(v) DMA stands for

a. Discrete Memory Access
b. Direct Memory Access
c. Discrete Memory Architecture
d. Direct Memory Architecture

(vi) Boolean algebra is also known as

a. Gate algebra
b. Transistor algebra
c. Switching algebra
d. Counting algebra

(vii) Convert the binary number (1111000011110000) to hexadecimal number

a. 1010
b. F0F0
c. 7070
d. 5050

(viii) The address line required for 16 k byte memory chip are

a. 13
b. 14
c. 15
d. 16

(ix) Which of the following is a user programmable register?

a. Memory Address Register
b. Accumulator
c. Program Counter
d. All of these

(x) 2's Complement of 10101011 is

a. 01010101
b. 11010101
c. 01110101
d. 01011101

Group – B

(Short Answer Type Question) 3 x 5 = 15

Answer any *three* from the following

2. Describe Harvard Architecture. [5]
3. Differentiate between Fixed Point and Floating Point Number. [5]
4. (a) What is Programmed IO? [3]
   (b) What are the different types of interrupts? [2]
5. What are the advantages and disadvantages of Asynchronous BUS? [5]
6. Explain Locality of Reference. [5]

Group – C

(Long Answer Type Question) 3 x 15 = 45

Answer any *three* from the following

7.	(a)	What do you mean by Von Neumann architecture?	[5]
	(b)	Discuss bottleneck of Von Neumann's Architecture.	[4]
	(c)	What are the different pipeline hazards?	[6]
8.	(a)	Multiply – 4 and 3 using Booth's Multiplication Algorithm.	[8]
	(b)	Explain the functionality of DMA Controller with proper diagram.	[7]
9.	(a)	What are the two different ways of writing in cache memory? Explain briefly.	[5]
	(b)	Differentiate between RISC and CISC.	[5]
	(c)	X and Y are two consecutive numbers in a number system. If $XY=(39)_{10}$ and $YX= (33)_{10}$ then find the value of X and Y.	[5]
10.	(a)	Explain Flynn's classification.	[7]
	(b)	Calculate total miss if hit is 2.0 and hit ratio is 0.33.	[3]
	(c)	Find 2's compliment of $(1AB)_{16}$.	[2]
	(d)	Convert $(78.96)_{10}$ into Octal.	[3]
11.		Write short notes on (any three)	[3X5=15]
	(a)	DMA	[5]
	(b)	Universal Gate	[5]
	(c)	De Morgan's Theorem	[5]
	(d)	1's and 2's Complement	[5]
	(e)	Memory Hierarchy	[5]
