BRAINWARE UNIVERSITY

Term End Examination 2018 - 19

Programme – Bachelor of Science (Honours) in Computer Science

Course Name - Computer Architecture and Organization

Course Code - BCS302

(Semester – 3)

Time allotted: 3 Hours **Full Marks : 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Question) 10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) Effective addressing refers to

a. the information from which the memory address of the operand can be determined.
b. the operand or its address explicitly, to determine the address of an operand
c. a data. that defines the actual location of a memory element
d. a memory portion, that defines the recent addresses

(ii The elementary components of a single DRAM cell are

a. 6 transistors
b. 2 transistors and one capacitor
c. 2 transistors and 2 inverters
d. 1 transistor and a capacitor

(iii) Main advantages of associative memory is

a. cheap in cost
b. they are built with semiconductors
c. suitable to store data rapidly
d. they are suitable for parallel searches due to its organization

(iv) Function of a program control unit is

a. it's function is to fetch instructions from memory and interrupt them
b. it's function is to fetch program from memory and process them
c. it's function is to fetch data from memory and use them
d. it's function is to count program and use them for the next process

(v) In IEEE floating point representation, extra bits of mantissa are called?

a. Guard bits.
b. Sign bits.
c. Carry bits.
d. Borrow bits.

(vi) A size of 512X8 RAM type memory chip will constructs with

a. 8 bit address bus and 8 bit data bus.
b. 512 bit address bus and 8 bit data bus.
c. 8 bit data bus and 9 bit address bus.
d. 512 bit data bis and 9 bit address bus.

(vii) What are the use of general purpose registers?

a. to store general input bits and intermediate data bits
b. to store cache elements and hit ratio information
c. to store data and intermediate results during the execution of a program
d. to store carry bits, and propagate the bits to carry flag register

(viii) The term clock cycle may refer to

a. a clock pulse.
b. an instruction cycle.
c. a data.
d. a single electronic pulse of a CPU.

(ix) Main disadvantage of Optical disks over magnetic storage is

a. optical disks are bigger in size
b. optical disks are expansive
c. optical disks have slower seek-times and transfer rates than magnetic media
d. optical disks have lower storage capacity.

(x) Carry look ahead adder (CLA) works faster than other adders, because

a. it adds more than two numbers.
b. it adds two numbers serially.
c. it adds two numbers without depending on the carry bits from the previous stages.
d. it adds only carry bits.

Group – B

(Short Answer Type Questions) 3 x 5 = 15

Answer any *three* from the following

2. What are the advantages of having different addressing modes in a computer architecture? Explain Implied Mode and Immediate Mode with example. 3+2

3. Why frequent refreshing is necessary for DRAM type memory? Describe a typical DRAM memory cell with necessary logic diagram. 2+3

4. Construct a basic ALU having 4 arithmetic operations and 4 logical operations. To identify any one of these four logical operations or four arithmetic operations, there are two control lines are needed. Also to identify the any one of these two groups- arithmetic or logical, another control line is needed. Show that, with the help of three control lines, any one of these eight operations can be performed. 5

5. Compare Structural Hazards and Data Hazards with suitable examples. 5

6. With necessary circuit diagram, design a 4-stage carry look-ahead adder (CLA) 5

Group – C

(Long Answer Type Questions) 3 x 15 = 45

Answer any *three* from the following

7 (a) Construct a 1K X 16 large RAM type memory with 512 X 8 RAM chips. 5

(b) Construct a 1K X 8 large RAM type memory with 512 X 4 RAM chips. 5

(c) Describe the working principle a typical CMOS SRAM type memory cell with necessary circuit diagram. 5

8.	(a)	A memory sub system has with a hierarchical cache memory-main has cache access time of 60 nsec., main memory access time of 120 nsec. and an overall hit ratio of 0.12. Calculate efficiency of the memory system.	8
	(b)	A three level memory system having cache access time of 5 nsec, and disk access time of 40 nsec, it has a cache hit ratio of 0.96 and the main memory hit ratio of 0.9. what should be the main memory access time to achieve an overall access time of 16 nsec?	7
9.	(a)	To show how the number of addresses affects a computer program, we can evaluate the arithmetic statement X= (A+B) – (C+D)Using zero, one, two or three address instructions.	8
	(b)	Represent decimal number 210.25_{10} in IEEE 754 floating point format.	7
10.	(a)	Show the bus connection with a CPU to connect four RAMs of size 256 X 8 bits each and a ROM of size512 X 8 bit in size. Assume that the CPU has 8 bit data bus and 16 bit address bus	8
	(b)	Compare SRAM with DRAM.	2
	(c)	Why DRAM type memory needs frequent refreshment ?	5
11.		Write short notes on any ***three***	
	(a)	Instruction length	5
	(b)	Serial adder and its application	5
	(c)	Optical storage	5
	(d)	RISC and CISC	5
