BRAINWARE UNIVERSITY

Term End Examination 2018-19

Programme – B.Tech. in Computer Science & Engineering

Course Name - Digital Electronics

Course Code – BCSE301

(Semester – 3)

Time allotted: 3 Hours **Full Marks: 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Question) 10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) The number of select input lines in 16X1 Multiplexer is

a. 8 b. 8

c. 4 d. 4

(ii) Total number of minterms using in Boolean variables is

a. n-1 b. n

c. 2^n d. 2^{n-1}

(iii) Popular application of flip-flop are?

a. Counters. b. Counters.

a. Registers. c. Transfer registers.

(iv) To implement Modulus 19 counter ,total number of JK flip flop will be

a. 5 b. 5

c. 3 d. 3

(v) The 2's complement of $(1101\ 0011)_2$ is

a. 0010 1101 b. 0010 1101

c. 0010 1100 d. 0010 1100

(vi) On a master-slave flip-flop, when is the master enabled?

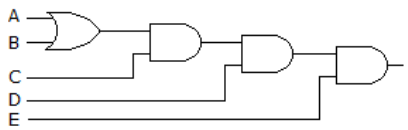
a. When the gate is LOW b. When the gate is HIGH

c. Both of the above d. Neither of the above

(vii) $(A5)_{16} = (X)_{10}$?

a. 140. b. 150.

c. 155. d. 165.

(viii) 

a. $[[C(A+B)D]E^{/}]$ b. $[C(A+B)D+E^{/}]$

c. C(A+B)DE d. ABCDE

(ix) How many address bits are needed to select all memory locations in the 2118 16K × 1 RAM?

a. 8. b. 14.

c. 10. d. 16.

(x) How many flip-flops are required to make a MOD-32 binary counter?

a. 3. b. 45.

c. 6. d. 5.

Group – B

(Short Answer Type Questions) 3 x 5 = 15

Answer any *three* from the following

2. Draw the block diagram for the circuit of 16 to 1 MUX by using two 74HC151. [5]
3. Draw the truth table and the logic circuit for 3 to 8 decoder. [5]
4. (a) What is the function of a D flip-flop that triggers only on positive-going transitions [3]
   (b) Explain with an example by drawing waveforms. [2]
5. (a) Differentiate latch and flip-flop. [2]
   (b) Draw a diagram and specify rise time, fall time and duration (width) of the pulse. [2]
   (c) What is NGT and PGT? [1]
6. Draw a 2's complement circuit and test with an example. [5]

Group – C

(Long Answer Type Questions) 3 x 15 = 45

Answer any *three* from the following

7. (a) Draw the circuit diagram of a clocked J-K flip-flop using only two input NAND gates. [5]
   (b) Implement $Y= (AB)^{/} +A+(B+C)^{/}$ only using NAND gates. [5 + 5]
   Realize $Y=(A+C)(A+D^{/})(A+B+C^{/})$ using NOR gates.

8. (a) Draw the truth table and circuit for 1 to 8 demultiplexer. [5]

(b) The logic expression of the output of a four input digital circuit is given bellow.
$B_3 = \sum_m (8, 9, 10, 11, 12, 13, 14, 15)$
$B_2 = \sum_m (4, 5, 6, 7, 8, 9, 10, 11)$
$B_1 = \sum_m (2, 3, 4, 5, 8, 9, 14, 15)$
$B_0 = \sum_m (1, 2, 4, 7, 8, 11, 13, 14)$
Simplify the above expressions by using K map and draw the logic circuit using XOR gate only. [10]

9. (a) Generate the logic expressions of a 4-bit carry look ahead adder from the truth table of a full adder and draw the circuit diagram. [8+5]

(b) Comment on the advantage of carry look ahead adder over conventional non-look ahead parallel adder. [2]

10. (a) Design a 4-bit ripple counter with block diagram. [2]

(b) Draw the wave forms of the outputs depending on the input clock signal and describe the process briefly by drawing the truth table. [4+2+2]

(c) Comment on the frequency division or frequency scaling of the above designed ripple counter. [3]

(d) Why it is called a MOD – 16 ripple counter? [2]

11. (a) Define uni-directional, bi- directional and Universal Shift Register? [3]

(b) Draw the circuit diagram of a 4 – bit Universal Shift Register and describe the operation with the help of function table. [8+4]
