BRAINWARE UNIVERSITY

Term End Examination 2018 - 19

Programme – Bachelor of Technology in Computer Science & Engineering

Course Name – Computer Architecture and Organization

Course Code – BCSE 303

(Semester - 3)

Time allotted: 3 Hours **Full Marks: 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Questions) 10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) Program Counter (PC) uses which of the following addressing mode?

a. Direct addressing mode
b. Relative addressing mode
c. Register addressing mode
d. All of these

(ii) The fastest data access is provided using _____

a. Cache Memory
b. Primary Memory
a. DRAMS
c. Registrar

(iii) Which of the following addressing modes permits relocation without any change whatsoever in the code?

a. Indirect addressing
b. Indexed addressing
c. Base register addressing
d. PC relative addressing

(iv) An interrupt in which the external device supplies its address as well as the interrupt requests is known as

b. Vectored interrupt
c. Maskable interrupt
d. Non maskable interrupt
e. Designated Interrupt

(v) The ability to temporarily halt the CPU and use this time to send information on buses is called

a. Direct memory access
b. Vectoring the interrupt
c. Polling
d. Cycle stealing

(vi) The principle of locality of references justifies the use of

a. Virtual memory
b. Main memory
c. Interrupts
d. Cache memory

(vii) Which of the following cycle is required to fetch and execute instruction?

a. Clock cycle
b. Process Life cycle
c. Instruction cycle
d. Memory cycle

(viii) Which of the following remarks about bit-slice processor is correct?

a. It can be cascaded to get any desired word length processor
b. It can be cascaded to get any desired word length processor
c. It does not contains anything equivalent of a program counter in a normal microprocessor
d. It does not contains anything equivalent of a program counter in a normal microprocessor

(ix) What of the following interrupt can be temporarily ignored by the processor?

a. Vectored interrupt
b. Non maskable interrupt
c. Maskable interrupt
d. Low priority interrupt

(x) The device which is used to connect a peripheral to bus is known as

a. Control register
b. interface
c. Communication protocol
d. None of these

Group – B

(Short Answer Type Questions) 3 x 5 = 15

Answer any *three* from the following

2. What do you mean by Addressing modes? Explain Immediate ,Register direct and Register indirect Addressing mode, [2+3]

3. Explain the instruction fetch and Instruction execution phase of an instruction with proper control signals. [3+2]

4. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. How many selection inputs are there in each multiplexer? What size of multiplexers are needed? How many multiplexers are there in the bus? [2+2+1]

5. What is the usage of the mode field in the instruction format? How mode field is related with the number of different addressing modes? [3+2]

6. What is DNA operator? Explain cycle stealing DNA. [2 + 3]

Group – C

(Long Answer Type Questions) 3 x 15 = 45

Answer any *three* from the following

7. (a) What do you mean by the term Virtual Memory? [5]

   (b) A virtual memory has page size of 1K words. There are eight pages and four blocks. The associative memory page table contains the following entries:

Page	Block
0	3
1	1
4	2
6	0

   Make a list of all virtual addresses (in decimal) that will cause a page fault if used by the CPU. [10]

8. (a) How many 128X8 RAM chips are needed to provide a memory capacity of 2048 bytes? [5]

   (b) How many lines of the address bus must be used to access 2048 bytes of memory? [5]

   (c) How many of these lines will be common to all chips? [5]

9. (a) Why Cache memory is used in Computer? [5]

(b) A digital computer has a memory unit of 32GB and a cache memory of 32KB. The cache uses the direct mapping technique with a block size of 1KB. Assume that the memory is byte addressable. Find the following:
How many bits are there in the tag, line number and block offset field of the address format?
What is the size of the tag directory? [10]

10. (a) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one address instructions can be formulated? [5]

(b) Write a program to evaluate the arithmetic statement:

X=A-B+C*(D*E-F)

Using a general register computer with three address instructions.

Using a general register computer with two address instructions.

Using an accumulator type computer with one address instructions.

Using a stack organized computer with zero-address operation instructions. [2.5+2.5+2.5+2.5]

11. A bus organized CPU has 16-registers with 32-bits in each, an ALU, and a destination decoder.

(a) How many multiplexers are there in the A bus and what is the size of each multiplexer? [3]

(b) How many selection inputs are needed for MUX A and MUX B? [3]

(c) How many inputs and outputs are there in the decoder? [3]

(d) How many inputs and outputs are there in the ALU for data, including input and output carries? [3]

(e) Formulate a control word for the system assuming that the ALU has 35 operations. [3]
