

BRAINWARE UNIVERSITY

Term End Examination 2019 - 20

Programme – Master of Science in Computer Science

Course Name – Advanced Computer Architecture

Course Code - MCS301

(Semester - 3)

Time allotted: 3 Hours Full Marks: 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group -A

(Multiple Choice Type Question) $20 \times 1 = 20$ 1. Choose the correct alternative from the following (Answer any Twenty) (i) Boolean algebra is also known as a. Counting algebra b. Switching algebra c. Transistor algebra d. Gate algebra If the searched data is found in the desired memory, it is said to be (ii) a. hit ratio b. miss d. hit rate c. hit (iii) The fastest data access can be obtained using a. SRAM b. DRAM c. Cache d. Register Which of the following is used to store intermediate result? (iv) b. MAR a. Accumulator c. MDR d. Program Counter DMA stands for (v) a. Discrete memory b. Discrete memory access architecture c. Direct memory architecture d. Direct memory access The method which offers higher speeds of I/O transfers is (vi) a. interrupts b. memory mapping

d. direct memory access

c. program controlled I/O

(vii)	Booth's	s algorithm is used for performing	bin	nary			
	a.	addition	b.	multiplication			
	c.	division	d.	subtraction			
(viii)	Which	is a part of Flynn's classification?					
	a.	MIMD	b.	SISD			
	c.	MISD	d.	all of above			
(ix)	In half subtractor, the difference circuit is implemented using						
	a.	XOR	b.	OR			
	c.	AND	d.	NOT			
(x)	The feature of RAM that makes it not suitable for permanent storage						
	a.	Slow	b.	volatile			
	c.	unreliable	d.	bulky			
(xi)	Which of the following has smallest capacity?						
	a.	cache memory	b.	RAM			
	c.	secondary memory	d.	registers			
(xii)	Write Through technique used in which memory for updating the data?						
	a.	Virtual memory	b.	Cache memory			
	c.	Main memory	d.	Auxiliary memory			
(xiii)	Virtual	memory consists of					
	a.	SRAM	b.	DRAM			
	c.	Magnetic memory	d.	None of these			
(xiv)	Memory unit accessed by content is called						
	a.	ROM	b.	Virtual memory			
	c.	Programmable memory	d.	Associative memory			
(xv)	MIMD	stands for					
		Multiple instruction	b.	Memory instruction multiple data			
		multiple data Multiple instruction	d	Multiple information multiple data			
		memory data	u.	Multiple information multiple date			
(xvi)	An interface that provides a method for transferring binary information between						
		l storage and external devices is ca					
		I/O interface		Input interface			
(::\		Output interface		I/O bus			
(xvii)	If the value $V(x)$ of the target operand is contained in the address field itself, the addressing mode is						
		Immediate	b.	direct			
	C.	indirect	d.	implied			

(xviii)	and pe	An interface that provides I/O transfer of data directly to and from the memory unit and peripheral is termed as						
	a.	DDA	b.	Serial interface				
	c.	BR	d.	DMA				
(xix)	_	A register capable of shifting its binary information either to the right or the left is called a						
	a.	parallel register	b.	serial register				
	c.	shift register	d.	storage register				
(xx)	SISD	stands for						
	a.	Single instruction single data	b.	Single information single data				
	c.	data		Single instruction sequence data				
(xxi)	Run ti	Run time mapping from virtual to physical address is done by						
	a.	memory management unit	b.	CPU				
	c.	PC	d.	none of above				
(xxii)	A mer	A memory used to store frequent used data						
	a.	stack pointer	b.	accumulator				
	c.	cache	d.	disk buffer				
(xxiii)) Cache	Cache memory-						
	a.	has greater capacity than RAM		is faster to access than CPU Registers				
	c.	is permanent storage	d.	faster to access than RAM				
(xxiv)) The ac	ddressing mode, where the ope	erand valu	ie is implicitly specified				
	a.	implied	b.	direct				
	c.	immediate	d.	indirect				
(xxv)	Virtua	Virtual memory is –						
	a.	an extremely large main memory	b.	an extremely large secondary memory				
	c.	an illusion of an extremely large memory	d.	None of these				
		Gro	oup – B					
		(Short Answe	er Type (Questions) $4 \times 5 = 20$				
Answ	er any fo	<i>ur</i> from the following						
	• •	C	Computer	Organization and Computer 5				
	Architect		- 0p ato1					
3.	What is p	pipelining? What are the types	of pipelir	ning? 5				
	What is o	hat is cache memory? Write the difference between static RAM and dynamic 2+3 AM.						
5.	Explain t	xplain the concept of ripple carry adders.						

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6.	6. Differentiate between fixed point and floating point numbers.									
7.	Exp	lain carry look ahead adder.	5							
	Group – C									
		(Long Answer Type Questions)	$3 \times 10 = 30$							
Ans	wer a	ny three from the following								
8.		Multiply 8 and 4 using booth's algorithm.	10							
9.		What are the different stages of an instruction cycle?	10							
10.	(a)	What is propagation delay?	2							
	(b)	How it can be reduced in carry look ahead adder? Explain with suitable	8							
		diagram.								
11.	(a)	What is coherence property in memory organization?	2							
	(b)	Explain the two methods used for coherence property.	8							
12.		Multiply -3 and 4 using booth's algorithm.	10							