



BRAINWARE UNIVERSITY

Term End Examination 2024-2025

Programme – M.Tech.(RA)-2024

Course Name – Electronics In Robotic Technology

Course Code - MEC10302A

(Semester I)

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Brainware University
398, Ramkrishnapur Road, Barasat
Kolkata, West Bengal-700125

Full Marks : 60

Time : 2:30 Hours

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question)

1 x 15=15

1. Choose the correct alternative from the following :

- (i) State the sequential logic circuits from of the following. 1.Full adder 2. Full subtractor 3. Half adder 4. J-K flip 5. Counter
- a) 1 only
b) 3 and 4
c) 4 and 5
d) 1, 2 and 3
- (ii) The output Q_n of a J-K flip-flop is 1. It changes to 0 when a clock pulse is applied. The input J_n and K_n are evaluated as
- a) 0 and X
b) '1 and X
c) X and 1
d) X and 0
- (iii) A BJT with forward current transfer ratio $\alpha = 0.98$, when working in CE mode, calculate current transfer ratio β .
- a) 98
b) 0.02
c) 49
d) 0.49
- (iv) Show, An operational amplifier possesses
- a) Very large input resistance and very large output resistance
b) Very large input resistance and very small output resistance
c) Very small input resistance and very small output resistance
d) Very small input resistance and very large output resistance
- (v) An operational amplifier has an open-loop gain of 200,000. Its output exhibits saturation at 10V. Calculate the threshold differential voltage of the amplifier
- a) 25 μ V
b) 50 μ V
c) 0.5 mV
d) 10V
- (vi) Find, if a JFET operates above pinch-off voltage,
- a) Drain current remains constant
b) Drain current increases rapidly
c) Drain current decreases gradually
d) Depletion region becomes zero
- (vii) A JFET has a value of $g_{m0} = 4000 \mu S$. Calculate the value of g_m at $V_{GS} = -3V$. Given that $V_{GS}(\text{off}) = -8V$.

- a) 2 micro Second
c) 20 micro second
- (viii) Choose the correct Option: If the input is a rectangular pulse, the output of an integrator is
a) Sine wave
c) Ramp
- (ix) Indicate when, for a JFET, drain current is maximum.
a) when VGS is zero
c) when VGS is positive
- (x) In D flip-flop, D is indicated as
a) Distant
c) Desired
- (xi) Write, the transfer of a signal in a transistor is
a) low to high resistance
c) collector to base junction
- (xii) The cut-in-voltage for gallium arsenide is
a) 1.2 V
c) 0.7 V
- (xiii) Choose from the following a part of a BMS that ensures the safety of the battery pack.
a) Charging circuit
c) Protection circuit
- (xiv) Select a flyback converter that is commonly used for:
a) Low power applications
c) Medium power applications
- (xv) Choose the 7912 regulator that provides:
a) +12V
c) +5V
- b) 200 micro second
d) 2000 micro second
- b) Square wave
d) Rectangular wave
- b) when VGS is negative
d) when VGS is equal to pinch-off voltage
- b) Data
d) Delay
- b) High to low resistance
d) Emitter to base junction
- b) 0.3 V
d) None of these
- b) Monitoring circuit
d) Discharge circuit
- b) High power applications
d) Ultra-high power applications
- b) -12V
d) -5V

Group-B

(Short Answer Type Questions)

3 x 5=15

2. Illustrate the advantages of MOSFET. (3)
3. Write characteristics of an ideal op-amp. (3)
4. In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 μ A. Identify the total collector current. Given that $\alpha = 0.92$. (3)
5. Explain the charging process in a BMS. (3)
6. Explain 1:2 De-multiplexer through block diagram, truth table, logical expression and circuit diagram. (3)
- OR
- Explain 2:4 Decoder through block diagram, truth table, logical expression and circuit diagram. (3)

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Group-C
(Long Answer Type Questions)

5 x 6=30

7. Describe the I-V characteristic of MOSFET. (5)
8. Explain the Summing Amplifier developed by OP-AMP. (5)
9. Given $CMRR = 10^5$ and differential gain $= 10^5$, Calculate for the common mode gain of the OPAMP. (5)
10. Explain the construction of transistor with diagram. (5)
11. Explain a flyback converter and its operation. (5)
12. Explain the Construction of 8:1 multiplexer using 4:1 multiplexer and OR gate. (5)

OR

- Explain the Construction of 16:1 multiplexer using 4:1 multiplexer only. (5)

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