BRAINWARE UNIVERSITY

Term End Examination 2024-2025
Programme – MCA-2024
Course Name – Computer Organization and Architecture
Course Code - MCA17104 (T)
(Semester I)

Full Marks : 40 **Time : 2:0 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 10=10

1. *Choose the correct alternative from the following :*

(i) Find, which law is represented by A + A = A.
a) Idempotent Law b) Associative Law
c) Distributive Law d) Absorption Law

(ii) The expression A'B + AB' represents which logic gate?
a) AND b) OR
c) XOR d) NAND

(iii) Relate the circuit used to add two 1-bit binary numbers.
a) Decoder b) Multiplexer
c) Full adder d) Half adder

(iv) Classify which of the following is a sequential circuit.
a) Half adder b) Full adder
c) Flip-flop d) Encoder

(v) Choose the example of a non-volatile memory from the following.
a) RAM b) ROM
c) Register d) Cache

(vi) Demonstrate the output of a JK flip-flop when both J and K are high.
a) Resets b) Sets
c) Toggles d) Remains unchanged

(vii) Infer the issue solved by a master-slave flip-flop.
a) Race around conditions b) Timing issues
c) Power loss d) Data overflow

(viii) Estimate how many output combinations a 3-input AND gate can have.
a) 4 b) 6
c) 8 d) 16

(ix) Which addressing mode involves specifying the address of a memory location indirectly through a register?

a) Immediate Addressing
b) Register Addressing
c) Direct Addressing
d) Indirect Addressing

(x) Identify the component responsible for executing instructions and performing required operations.

a) ALU
b) Control Unit
c) Program Counter
d) Instruction Register

Group-B
(Short Answer Type Questions) 3 x 5=15

2. Infer pipelining organization in brief. (3)
3. Explain the concept of memory hierarchy. (3)
4. Difference between Synchronous bus and asynchronous bus. (3)
5. What is meant by the term stored program concept? (3)
6. Difference between RISC & CISC architecture. (3)

OR

Propose the usability of MAR & MDR. (3)

Group-C
(Long Answer Type Questions) 5 x 3=15

7. Define the process of simplifying a Boolean expression using a Karnaugh Map (K-Map). (5)
8. Examine "Data hazards can be resolved in pipelined architectures". (5)
9. Explain the toggle behavior of the JK flip-flop. (5)

OR

Defend Race Around Condition. (5)

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