BRAINWARE UNIVERSITY

Term End Examination 2024-2025
Programme – Dip.RA-2022/Dip.RA-2023
Course Name – Digital Electronics
Course Code - ECPC303
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select the decimal equivalent of hex number 1A53-
a) 6793 b) 6739
c) 6973 d) 6379

(ii) Identify the decimal equivalent of the octal number 140-
a) 96 b) 86
c) 90 d) none of these

(iii) Identify Octal equivalent number of decimal number 345-
a) 135 b) 531
c) 153 d) 532

(iv) Select 2's complement of the number 1101110 is-
a) 10001 b) 10001
c) 10010 d) None of these

(v) The gray code of the binary number 100101 is recognized as-
a) 101101 b) 1110
c) 110111 d) 111001

(vi) Select the two inputs of The NOR gate when output will be high-
a) 0 b) 1
c) 10 d) 11

(vii) Power consumption of CMOS circuits is indicated as-
a) Equal to TTL b) Less than TTL
c) Twice of TTL d) Thrice of TTL

(viii) Determine the number of cells in a 6-variable K-map.
a) 6 b) 12
c) 36 d) 64

(ix) Karnaugh map is chosen for the purpose of-
a) Reducing the electronic circuits used b) To map the given Boolean logic function

c) To minimize the terms in a Boolean expression
d) To maximize the terms of a given a Boolean expression

(x) The gates required to construct a half adder are

a) EX-OR gate and NOR gate
b) EX-OR gate and OR gate
c) EX-OR gate and AND gate
d) EX-OR gate and NAND gate

(xi) Exclusive-OR (XOR) logic gates can be constructed from what other logic gates namely-

a) OR gates only
b) AND gates and NOT gates
c) AND gates, OR gates, and NOT gates
d) OR gates and NOT gates

(xii) Determine the number of select lines to construct a 8 – to – 1 multiplexer-

a) 2
b) 3
c) 4
d) 5

(xiii) Choose the output from the following for a 1:4 demultiplexer, if the two control inputs are C1 = 1 & C2 = 1.

a) Y0
b) Y1
c) Y2
d) Y3

(xiv) Identify how many NAND gates required to implement a OR gate-

a) 1
b) 2
c) 3
d) 4

(xv) Each term in the standard POS form is illustrated as-

a) minterm
b) maxterm
c) don't care
d) none of these

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Explain D flip-flop with its truth table, circuit diagram and working principle. (3)

3. Apply K-map to simplify the following expression (3)
F(A,B,C,D)= Σ m (0,1,2,3,7,8,9,10,11,14).

4. Explain SOP and POS. (3)

5. Describe AND, OR and NOT gates with its Boolean expression, truth table and logical symbol. (3)

6. Construct half adder circuit by using logic gates. (3)

OR

Construct half subtractor circuit by using logic gates. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Design a full adder circuit using a 3 to 8 line decoder. (5)

8. Explain J-K flip-flop with its block diagram, circuit diagram and working principle. (5)

9. Describe logic family. Classify logic families with components used in the logic families. (5)

10. (a) Convert the binary number 10110 to the octal equivalent number system. (5)
    (b) Convert the hexadecimal number A3D to the binary number system.
    (c) Convert the octal number 26 to its hexadecimal equivalent number.

11. Explain the construction of D flip flop using S-R flip flop. (5)

12. Construct 8:1 multiplexer using 4:1 multiplexer and OR gate. (5)

OR

Construct 16:1 multiplexer using 4:1 multiplexer only. (5)

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