BRAINWARE UNIVERSITY

Term End Examination 2024-2025
Programme – B.Tech.(RA)-2022/B.Tech.(RA)-2023
Course Name – Digital System Design
Course Code - PCC-ECR302
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) The NAND gate output will be low if the two inputs are
a) 00 b) 01
c) 10 d) 11

(ii) Select the binary equivalent of the decimal number 368
a) 101110000 b) 110110000
c) 111010000 d) 111100000

(iii) Identify hexadecimal equivalent number of octal number 734
a) C 1 D b) D C 1
c) 1 C D d) 1 D C

(iv) The output of a logic gate is 1 when all its inputs are at logic 0. Identify the gate(s)-
a) a NAND or an EX-OR b) an OR or an EX-NOR
c) an AND or an EX-OR d) a NOR or an EX-NOR

(v) Find the 2's complement of the number 1101101 -
a) 101110 b) 111110
c) 110010 d) 10011

(vi) Select 2's complement of the number 1101110 is
a) 10001 b) 10001
c) 10010 d) None of these

(vii) When an input signal A=11001 is applied to a NOT gate serially, its output signal is represented as
a) 111 b) 110
c) 10101 d) 11001

(viii) The binary equivalent of hexadecimal number FA is indicated as
a) 1010 1111 b) 1111 1010
c) 10110011 d) none of these

(ix) Let the input of a subtractor is A and B; then determine the output if A = B.

a) 0 b) 1
c) A d) B

(x) Which of the following circuits are chosen under the class of sequential logic circuits?
1.Full adder 2. Full subtractor 3. Half adder 4. J-K flip 5. Counter

a) 1 only b) 3 and 4
c) 4 and 5 d) 1, 2 and 3

(xi) Choose the desired logic circuits which accept two binary digital on inputs and produces two binary digital, a sum bit and carry bit on its outputs?

a) full adder b) half-adder
c) serial adder d) parallel adder

(xii) Determine How many AND, OR and EXOR gates are required to design a full adder?

a) 1, 2, 2 b) 2, 1, 2
c) 3, 1, 2 d) 4, 0, 1

(xiii) Determine How many NOT gates are required for the construction of a 4-to-1 multiplexer?

a) 3 b) 4
c) 2 d) 5

(xiv) Which input values will cause an AND logic gate to produce a HIGH output?

a) At least one input is HIGH b) At least one input is LOW
c) All inputs are HIGH d) All inputs are LOW

(xv) A 4-variable AND-OR-Invert circuit produces a 0 at its Y output. Which combination of inputs is correct?

a) $\overline{A}B + \overline{C}D$ b) $\overline{A}\,\overline{B} + \overline{C}\,\overline{D}$

c) $\overline{A}\,\overline{B} + CD$ d) None of these

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Construct Ex-OR gate using NAND gates only. (3)

3. Apply K-map to simplify the following expression (3)

$Y(A, B, C, D) = \prod M(0,1,4,5,6,8,9,12,13,14)$ ..

4. State and explain De-Morgan's Law. (3)

5. Explain 1:2 De-multiplexer through block diagram, truth table, logical expression and circuit diagram. (3)

6. Construct 4:1 Multiplexer using three 2:1 Multiplexer. (3)

OR

Construct a 4 × 16 decoder using 3 × 8 decoder. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain the construction of D flip flop using J-K flip flop. (5)

8. Explain full subtractor through its block diagram, truth table, expression of the output and implement the full subtractor circuit using logic gates. (5)

9. Explain the construction of half adder using NAND gate and NOR gate. (5)

10. (5)

(a) Apply Boolean algebra to prove that $A \cdot \overline{C} + \overline{A} \cdot C = B$ if,
$A \cdot \overline{B} + \overline{A} \cdot B = C$

(b) Apply Boolean algebra to simplify the expression
$Y = \overline{A} \cdot B + A \cdot B + \overline{A} \cdot \overline{B}$

11. Construct 16:1 multiplexer using 4:1 multiplexer only. (5)

12. Design the following function using 8:1 multiplexer (5)
$F(A, B, C, D) = \sum m(0, 1, 3, 5, 8, 9, 11, 14, 15)$

OR

Design 4:16 decoder using 2:4 decoder. (5)

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