BRAINWARE UNIVERSITY

Term End Examination 2024-2025
Programme – B.Tech.(CSE)-DS-2021/B.Tech.(CSE)-DS-2022/B.Tech.(CSE)-DS-2023
Course Name – Computer Organization and Architecture/Computer Organization & Architecture
Course Code - PCC-CSD301
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Express the correct term for IEEE 32-bit representation of the decimal number.
   a) Double-precision b) Single-precision
   c) Extended format d) None of these

(ii) Identify the format that internal data storage in RAM uses
   a) Hexadecimal b) Octal
   c) Binary d) Decimal

(iii) Choose the base of the Hexadecimal number system
   a) 2 b) 8
   c) 10 d) 16

(iv) Identify the memory that loses its data when the power is switched off.
   a) Non-Volatile Memory b) Volatile Memory
   c) Both A and B d) None

(v) Identify the formula for the Hit Ratio
   a) Hit/(Hit + Miss) b) Miss/(Hit + Miss)
   c) (Hit + Miss)/Miss d) (Hit + Miss)/Hit

(vi) Explain the arithmetic left shift operation as
   a) Produces the same result as obtained with logical shift left operation
   b) Causes the sign bit to remain always unchanged
   c) Needs additional hardware to preserve the sign bit
   d) Needs additional hardware to preserve the sign bit

(vii) Explain the binary subtraction operation in a digital computer
   a) In the same way as we perform subtraction in decimal number
   b) Using 2's complement method
   c) Using 1's complement method
   d) Using 10's complement method

(viii) Interpret 2's complement representation of (-23)

a) 10111 b) 11011
c) 10100 d) 01001

(ix) Choose the component that is used for addition in ALU

a) Adder b) Subtractor
c) Multiplier d) By program only

(x) Identify the fastest data access memory

a) Cache b) DRAM's
c) SRAM's d) Registers

(xi) Select the memory that is independent of the address bus

a) Secondary memory b) Main memory
c) Onboard memory d) Cache memory

(xii) Select the non-volatile memory

a) RAM b) ROM
c) Cache d) ROM and Cache

(xiii) Select the input device

a) Keyboard b) Mouse
c) Scanner d) All of these

(xiv) Overlapping of stages is a concept of _____. Select the correct answer.

a) pipelining b) sequential processing
c) parallel processing d) All of these

(xv) Select the correct option that is/are type of pipelining

a) instruction b) arithmetic
c) Both of these d) none of these

Group-B

(Short Answer Type Questions) 3 x 5=15

2. State Von Neumann architecture with block diagram. (3)
3. Discuss the Write-Through and Write-Back cache write policies. (3)
4. Establish the performance measured in a pipeline processing. (3)
5. State the difference between PROM & EPROM. (3)

6. Estimate the easiest way to determine cache locations to search memory addresses. (3)

OR

Illustrate the difference between interrupt service routine and subroutines (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain Set-Associative mapping along with its advantage and disadvantage. (5)
8. Consider the page reference string 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 3 with 4 page frames. Write number of page faults using OPR (5)
9. Describe the different types of special purpose registers in details. (5)
10. Explain the advantages and disadvantages of the Booth multiplier in terms of speed and hardware complexity? (5)
11. Explain propagation delay of Ripple Carry Adder and how it can be reduced in Carry Look Ahead adder, explain with suitable block diagram (5)
12. Justify Locality of reference along with its types. (5)

OR

Justify the better page replacement algorithm among FIFO and LRU. (5)