BRAINWARE UNIVERSITY

Term End Examination 2024-2025
Programme – B.Tech.(CSE)-2023
Course Name – Computer Organization & Architecture
Course Code - PCC-CSG301
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify hexadecimal number equivalent to binary number (1111000011110000).
a) 1010 b) F0F0
c) 7070 d) 5050

(ii) Identify the format in which computer system usually store data.
a) Hexadecimal b) Octal
c) Binary d) Decimal

(iii) Identify the formula for Hit Ratio
a) Hit/(Hit Miss) b) Miss/(Hit Miss)
c) (Hit Miss)/Miss d) (Hit Miss)/Hit

(iv) Convert (100110)2 in octal
a) (46)8 b) (2A2)H
c) (36)10 d) (26)10

(v) Select the suitable memory that is independent of the address bus device.
a) Secondary memory b) Main memory
c) Onboard memory d) Cache memory

(vi) Select the fastest memory name in the computer memory hierarchy.
a) Cache b) Register in CPU
c) Main memory d) Disk cache

(vii) Identify the name of universal logic gate from the following options.
a) OR b) AND
c) XOR d) NAND

(viii) Select the memory management technique where the allocated size is fixed
a) paging b) segmentation
c) fragmentation d) indexing

(ix) Select the memory that has the highest access time.
a) Cache b) Registers

c) RAM d) Program Counter

(x) Select the functional block of a computer that performs arithmetic and logic operations

a) Memory b) Input-Output Subsystems
c) Control Unit d) ALU

(xi) Select the alternate name for structural hazard in pipelining

a) control hazard b) data hazard
c) resource hazard d) program hazard

(xii) Express the term that represent periods of time when the unit is idle _____

a) Stalls b) Bubbles
c) Hazards d) Both Stalls and Bubbles

(xiii) Identify the reason for which pipeline conflict occurs in pipelined processor.

a) Instruction Dependency b) Data dependency
c) Branch difficulties d) control dependency

(xiv) The transfer between CPU and Cache is expressed as _____.

a) Block transfer b) Word transfer
c) Set transfer d) Associative transfer

(xv) Select from the following that is not a form of memory.

a) instruction cache b) instruction register
c) instruction opcode d) translation lookaside buffer

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Demonstrate functions of cache memory with suitable diagram. (3)
3. Explain different performance parameters of pipeline architecture. (3)
4. Mention all the differences between computer organization and computer architecture. (3)
5. Explain De Morgan's Theorem. (3)
6. Illustrate the write-through method (3)

OR

Differentiate between associative and set associative mapping. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Consider the page reference string 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 3 with 4 page frames. Measure the number of page faults using LRU (5)
8. Describe the steps involved in the Instruction Execution Cycle. (5)
9. Explain parallel processing with suitable example. (5)
10. Explain memory hierarchy in computer systems with diagram. (5)
11. Summerize the key characteristics, uses, and performance differences between SRAM and DRAM. (5)
12. Explain the flowchart for Booth's multiplication algorithm. (5)

OR

Explain propagation delay of Ripple Carry Adder and can it reduced in Carry Look Ahead adder, explain with suitable block diagram (5)

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