BRAINWARE UNIVERSITY

Term End Examination 2024-2025
Programme – B.Tech.(CSE)-AIML-2021/B.Tech.(CSE)-AIML-2022/B.Tech.(CSE)-AIML-2023
Course Name – Computer Organization and Architecture/Computer Organization & Architecture
Course Code - PCC-CSM301
(Semester III)

Full Marks : 60

Time : 2:30 Hours

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question)   1 x 15=15

1. Choose the correct alternative from the following :

(i) Identify the main characteristic that distinguishes the Von Neumann architecture from other architectures:

a) Separate memory for data and instructions   b) Shared memory for data and instructions

c) Separate ALUs for arithmetic and logic operations   d) Dual CPUs for parallel processing

(ii) Identify the type of storage used in the Von Neumann architecture to hold the currently executing instruction:

a) Control Unit   b) Cache

c) Register   d) All of the above

(iii) Convert the binary number (1111000011110000) to hexadecimal number

a) 1010   b) F0F0

c) 7070   d) 5050

(iv) Identify what 32-bit representation of the decimal number is known as

a) Double-precision   b) Single-precision

c) Extended format   d) None of these

(v) Identify the register that holds the address of the next instruction to be executed in the Von Neumann architecture:

a) Accumulator   b) Program Counter (PC)

c) Instruction Register (IR)   d) Data Register (DR)

(vi) Show the number which is numerically equal to $(100110)_2$

a) $(46)_8$ b) $(2A2)_H$

c) $(36)_{10}$ d) $(26)_{10}$

(vii) Identify the correct example for Auxiliary Memory

a) Magnetic disks   b) Tapes

c) Flash memory   d) Both A and B

(viii) Explain the binary subtraction that is performed in a digital computer.

a) In the same way as we perform subtraction in decimal number
b) Using 2's complement method
c) Using 9's complement method
d) Using 10's complement method

(ix) Select the true statement about Adder-subtractor composite unit

a) It can add as well as subtract two numbers
b) At a time, it either adds or subtracts
c) It mainly operates with parallel adder
d) All of these

(x) Recognize in which all intermediate carry generated at first stage

a) CPA
b) CLA
c) Both
d) None of these

(xi) Write addition is done with the help of _____ in ALU

a) Adder
b) Subtractor
c) Multiplier
d) By program only

(xii) Select the fastest means of memory access for CPU determine

a) Registers
b) Cache
c) Main memory
d) Virtual Memory

(xiii) If M denotes the number of memory locations and N denotes the word size, then compute the storage capacity is _____.

a) M*N
b) M+N
c) 2M+N
d) 2M-N

(xiv) Identify which of the following is/are types of multiprocessors based on memory.

a) Shared memory
b) Distributed memory
c) Both of these
d) None of these

(xv) Choose among the following the structural hazard in pipelining as.

a) control hazard
b) data hazard
c) resource hazard
d) program hazard

Group-B
(Short Answer Type Questions)   3 x 5=15

2. Explain briefly how RTL interpretation is used to illustrate the transfer of data between registers.   (3)
3. Illustrate Ripple Carry Adder. State the disadvantage of it.   (3)
4. Explain the advantages of Static RAM Over Dynamic RAM   (3)
5. Explain cache mapping function, and why is it necessary?   (3)
6. Express the concept of throughput and how it relates to pipelining.   (3)

OR

Write the difference between shared memory and distributed memory architectures in parallel processing.   (3)

Group-C
(Long Answer Type Questions)   5 x 6=30

7. Illustrate about Microoperations   (5)
8. Explain the advantage of Associative mapping over diret mapping.   (5)
9. Explain the fixed and floating point representation of numbers.   (5)
10. Justify the data dependencies in pipelining?   (5)
11. Compare and distinguish the advantage and disadvantage of different cache mapping techniques with examples of scenarios where each mapping technique is allowed.   (5)
12. Summarize direct mapping along with its advantage and disadvantage.   (5)

OR

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Measure the number of page faults using LRU

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