BRAINWARE UNIVERSITY

Term End Examination 2024-2025
Programme – B.Tech.(RA)-2022
Course Name – VLSI Circuit Design
Course Code - PCC-ECR501
(Semester V)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Define VLSI.

a) A type of software program
b) A methodology for designing circuits
c) A type of processor architecture
d) A type of network protocol

(ii) Identify the meaning of "semiconductor" in the context of VLSI.

a) A material that conducts electricity well
b) A type of insulator
c) A material that resists the flow of electricity
d) A type of conductor

(iii) List the primary steps involved in transforming a circuit design into a physical layout.

a) Circuit optimization, circuit verification, physical design
b) Circuit verification, physical design, circuit optimization
c) Physical design, circuit optimization, circuit verification
d) Not any of these.

(iv) Compare the differences between Moore's Law and Dennard Scaling.

a) Moore's Law only applies to transistor count, while Dennard Scaling addresses transistor size and power consumption.
b) Moore's Law and Dennard Scaling both refer to the transistor count of integrated circuits.
c) Moore's Law and Dennard Scaling both focus on the power consumption of integrated circuits.
d) Moore's Law and Dennard Scaling are not related to VLSI design concepts.

(v) Identify the different levels of design abstraction in VLSI design.

a) Physical Design, Circuit Design, and System Design
b) RTL Design, Logic Synthesis, and Behavioral Design
c) Logic Synthesis, Physical Design, and System Design
d) Circuit Design, Physical Design, and Behavioral Design

(vi) Identify the steps involved in full custom design.

a) Design, implementation, verification, validation
b) Design, verification, implementation, validation
c) Design, implementation, validation, verification
d) Design, validation, implementation, verification

(vii) Identify the advantages of full custom design.

a) Higher performance, lower power consumption, smaller size
b) Lower performance, higher power consumption, smaller size
c) Higher performance, higher power consumption, larger size
d) Lower performance, lower power consumption, larger size

(viii) Associate the following design steps with the correct order.

a) Design, implementation, validation, verification
b) Design, verification, implementation, validation
c) Design, implementation, verification, validation
d) Design, validation, implementation, verification

(ix) Differentiate between standard cell and gate array designs.

a) Standard cell design is more flexible than gate array design.
b) Gate array design is more flexible than standard cell design.
c) Both standard cell and gate array designs are equally flexible.
d) Not any of these.

(x) Discuss the advantages of semi-custom design.

a) Lower NRE cost
b) Shorter design cycle time
c) Better performance
d) Not any of these.

(xi) Discover the step in wafer processing that involves creating an oxide layer on the wafer surface.

a) Schedule the oxidation process
b) Simulate the oxide layer formation
c) Establish the oxide layer thickness
d) Complete the oxide layer formation

(xii) Report the purpose of the photolithography process.

a) Prepare the wafer surface
b) Record the wafer thickness
c) Develop the oxide layer
d) Transfer the pattern onto the wafer

(xiii) Examine the purpose of the ion implantation process.

a) Collect the implanted ions
b) Relate the implantation dosage
c) Judge the implantation energy
d) Change the doping concentration

(xiv) Choose a process of removing material from the surface of a semiconductor wafer.

a) Oxidation
b) Diffusion
c) Etching
d) Cleaning

(xv) Choose a process used to remove contaminants and residues from the surface of a semiconductor wafer.

a) Diffusion
b) Epitaxial Deposition
c) Photo-lithography
d) Cleaning

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Explain the process of ion-implantation in VLSI fabrication. (3)
3. Examine the various processes involved in wafer processing for VLSI fabrication. (3)
4. Identify the basic idea behind VLSI. (3)
5. Identify the basic idea behind ULSI. (3)

6. Explain the difference between full custom and semi-custom FPGA design. (3)

OR

Explain the role of cell libraries in FPGA design. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Judge the impacts of VLSI chips on the semiconductor industry. (5)
8. Explain a clocked JK latch using CMOS technology. (5)
9. Explain how FPGA technology is used for hardware emulation. (5)
10. Predict the challenges arise during design of VLSI chips. (5)
11. Illustrate the way designers handle chip complexity. (5)
12. Anticipate the advantages and disadvantages of using silicon on insulator in CMOS technology. (5)

OR

Design a stick diagram for a simple VLSI circuit and explain the layout rules used. (5)

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