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BRAINWARE UNIVERSITY

Term End Examination 2024-2025
Programme – BCA-Hons-2024/BCA(MAWT)-Hons-2024
Course Name – Computer Organization
Course Code - VAC00016
(Semester II)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Register Transfer Language is primarily used to describe-
   a) The behavior of machine instructions in terms of internal data movement
   b) High-level programming syntax
   c) User commands in an operating system
   d) Cloud computing operations

(ii) What does the following register transfer notation indicate: R3 ← R1 + R2?
   a) The value of R1 is stored in R3
   b) The sum of R1 and R2 is stored in R3
   c) The value of R3 is moved to R1
   d) The sum of R2 and R3 is stored in R1

(iii) A microinstruction consists of:
   a) Machine code
   b) Control signals
   c) Addressing modes
   d) Memory operands

(iv) The major advantage of microprogrammed control is-
   a) Faster execution
   b) Easier modification
   c) Less hardware complexity
   d) Smaller instruction set

(v) In fixed-point representation, what does the "fixed" refer to?
   a) The value of the number
   b) The size of the memory allocated
   c) The speed of processing
   d) The position of the radix point

(vi) Convert the decimal number -5 to its 8-bit two's complement representation.
   a) answer is 00000101
   b) answer is 11111010
   c) answer is 11111011
   d) answer is 10000101

(vii) What is the exact scenario where Booth's algorithm would be most efficient?

a) Multiplying two small positive numbers.
b) Multiplying numbers with long sequences of 1s and 0s in the multiplier.
c) Multiplying a large positive number by a small positive number.
d) Multiplying two fractional numbers.

(viii) What is the purpose of asynchronous data transfer?

a) To increase CPU speed
b) To decrease memory latency
c) To handle devices with different speeds
d) To simplify arithmetic operations

(ix) How does priority interrupt resolve conflicts when multiple devices interrupt the CPU simultaneously?

a) By ignoring all interrupts
b) By delaying all interrupts
c) By serving interrupts based on their priority
d) By processing interrupts randomly

(x) What is the sequence of events during a DMA transfer?

a) CPU initiates the transfer, I/O device transfers data, CPU is notified upon completion.
b) I/O device transfers data, CPU handles each byte.
c) CPU transfers data directly, I/O device waits.
d) CPU initiates the transfer, I/O device transfers data.

(xi) What is the process of handling a page fault in a virtual memory system?

a) Data is retrieved from cache.
b) Data is discarded.
c) Data is retrieved from auxiliary memory and loaded into main memory.
d) CPU restarts.

(xii) Explain how a daisy-chaining priority interrupt system works.

a) All devices have equal priority.
b) CPU polls each device.
c) Devices send interrupt vectors.
d) Devices are connected in series, and the first device requesting an interrupt blocks others.

(xiii) What is vector processing?

a) Processing scalar data
b) Processing arrays of data simultaneously
c) Processing data using complex instructions
d) Processing data in a sequential manner

(xiv) What is the advantage of a RISC pipeline over a CISC pipeline?

a) Simpler pipeline stages
b) Variable instruction length
c) Complex instruction decoding
d) Microprogrammed control

(xv) What are the impact of pipeline depth on instruction throughput?

a) Deeper pipelines always increase throughput.
b) Shallow pipelines are always better.
c) Deeper pipelines increase throughput but increase hazard penalties.
d) Pipeline depth has no impact.

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Illustrate how a simple handshaking protocol can be used for asynchronous data transfer. (3)
3. Explain the instruction cycle in a basic computer, including the key steps involved. (3)
4. Differentiate between register transfer and bus transfer. Provide examples. (3)
5. Design a simple control unit sequence for a LOAD instruction. (3)
6. Explain shift micro-operations. How are they useful in computer processing? (3)

OR

Explain the difference between arithmetic and logic micro-operations. (3)

Group-C
(Long Answer Type Questions) 5 x 6=30

7. Explain the different types of instruction formats, including zero-address, one-address, two-address, and three-address formats, with examples. (5)
8. Describe the fundamental data types used in computer systems, including integer, floating-point, and character representations. For each type, list and explain the common formats and ranges, and provide examples of how these data types are used in programming. Discuss the significance of choosing the appropriate data type for a given application and how it affects memory usage and computational accuracy. (5)
9. Multiply 12 (multiplicand) by -5 (multiplier) using Booth's algorithm. Show all steps. What is the advantage of Booth's algorithm over standard multiplication for these numbers? (5)
10. Design an efficient interrupt handling mechanism for a system with multiple peripherals having varying priorities. Create a priority interrupt scheme that minimizes interrupt latency and ensures that high-priority interrupts are serviced promptly. Describe the hardware and software components required for your design, and explain how the system handles nested interrupts. (5)
11. Evaluate the architectural trade-offs between CISC and RISC processors in terms of performance, complexity, and power consumption. Analyze the impact of instruction set design on compiler efficiency and program execution speed. Justify which architecture would be more suitable for a modern embedded system with limited resources and stringent power constraints. (5)
12. Analyze the performance gains achieved by implementing an arithmetic pipeline for floating-point addition. Investigate the potential hazards that can arise in an arithmetic pipeline, such as data hazards and structural hazards. Propose strategies to mitigate these hazards and optimize the pipeline's throughput. (5)

OR

The evolution of computer architecture has led to two dominant paradigms: Complex Instruction Set Computing (CISC) and Reduced Instruction Set Computing (RISC). (a) Analyze the fundamental architectural differences between CISC and RISC, focusing on their instruction set complexity, addressing modes, and pipeline efficiency. (b) Subsequently, evaluate the trade-offs associated with each architecture in terms of performance, power consumption, and suitability for different application domains. Justify which architecture, in your opinion, offers a more advantageous design philosophy for modern computing needs, and explain the reasoning behind your choice. (5)

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