# BRAINWARE UNIVERSITY

**Term End Examination 2024-2025**
**Programme – Dip.CSE-2022/Dip.CSE-2023**
**Course Name – Computer Organization**
**Course Code - DCSE-PC401**
**( Semester IV )**

**Full Marks : 60** **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

## Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify the representation that uses one's complement for negative numbers.
   a) Binary Coded Decimal (BCD) b) Two's complement
   c) Gray code d) Excess-3 code

(ii) Select the correct character representation standard widely used in computers.
   a) ASCII b) EBCDIC
   c) Unicode d) Baudot Code

(iii) express floating-point representation as
   a) A representation where the position of the binary point is fixed b) A representation using only integers
   c) A representation with a floating binary point d) A representation with variable-length bits

(iv) Identify from the following is the example of Universal logic gate
   a) NAND b) XOR
   c) OR d) AND

(v) State RAM is called DRAM When
   a) It is alwayes moving around data b) It requirqs periodic refreshing
   c) It can do several things simulteneously d) None of this

(vi) Identify the division technique that restores the dividend after each subtraction.
   a) Restoring Division b) Non-Restoring Division
   c) Shift Division d) Booth Division

(vii) Select the correct statement about the Booth Multiplier.
   a) It is a non-restoring division technique b) It is used for addition only
   c) It reduces the number of partial products in multiplication d) It uses only fixed-point representation

(viii) Identify the primary function of a Common Bus System in ALU and CU Organization.

a) Facilitating communication between different components
b) Storing data temporarily
c) Performing arithmetic operations
d) Managing power consumption

(ix) Identify the role of the Logical and Shifter Unit in ALU and CU Organization.

a) Performing arithmetic operations
b) Handling logical AND, OR, and XOR operations
c) Managing control signals
d) Controlling the clock speed

(x) Select the advantage of using a parallel adder over a serial adder.

a) Lower power consumption
b) Simplicity in design
c) Faster computation
d) Improved data security

(xi) Select the characteristic of a parallel adder.

a) Processes one bit at a time
b) Requires fewer resources
c) Handles multiple bits simultaneously
d) Utilizes a shifter unit

(xii) Show the operational differences between Hardwired and Microprogrammed Control Unit designs.

a) Hardwired uses stored control memory, while Microprogrammed uses fixed logic circuits
b) Hardwired uses fixed logic circuits, while Microprogrammed uses stored control memory
c) Both use stored control memory
d) Neither uses stored control memory

(xiii) Select the full form of RISC.

a) Reduced Instruction set computer
b) Received computing set computting
c) Reducing Instruction set computer
d) Recycle computing set computting

(xiv) State the correct option for MAR

a) Memory address register
b) Memory access register
c) .None
d) .Both

(xv) Select the Operation of memory transfer:

a) Read
b) Write
c) Both
d) None

## Group-B

(Short Answer Type Questions) 3 x 5=15

2. Explain the types of addressing mode. (3)
3. Explain the Register Transfer Language (RTL) representation in the context of ALU and CU organization, and provide an example illustrating its application. (3)
4. Explain the Booth multiplier algorithm. (3)
5. Compare Von Neumann architecture with Harvard architecture. (3)
6. Explain the advantages of Static RAM Over Dynamic RAM (3)

**OR**

Explain the working principle of virtual memory in modern computer system. (3)

## Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain the architecture of a basic Computer. (5)
8. A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate. Then estimate the total time taken to process 1000 data items on the pipeline. (5)
9. Illustrate the operational differences between Hardwired and Microprogrammed Control Unit designs, and discuss their respective advantages and disadvantages. (5)
10. Summarize the different types of hazards in pipelining (5)

11. Identify the key differences between fixed-point and floating-point representations, providing examples to illustrate their application in computer arithmetic. (5)
12. Explain the performance of cache in computer architecture? (5)

**OR**

Explain direct memory access. (5)

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