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Term End Examination 2024-2025
Programme – B.Tech.(RA)-2022
Course Name – Nano Electronics
Course Code - PEC-ECR601B
(Semester VI)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify the element with one dimension in Nano range and the other two dimensions in large range
   a) Micro-material b) Quantum wire
   c) Quantum well d) Quantum dot

(ii) Select the condition of the melting point of particles in nano form
   a) Increases b) Decreases
   c) Remains same d) Increases then decreases

(iii) Identify the processes of materials was not described as Nanotechnology
   a) Separation b) Creation
   c) Processing d) Consolidation

(iv) Express the main issue obtained in system integration related to interconnects
   a) Decreasing interconnect resistance b) Increasing interconnect capacitance
   c) Decreasing interconnect length d) Increasing interconnect delay

(v) Identify that the short channel effect is resulting from
   a) small drain depletion region b) change in electron drift characteristics
   c) depletion charge sharing between the gate , the source and the drain d) None of these

(vi) Indicate which one does not minimize punch-through
   a) long channel b) weaker substrate doping
   c) thinner oxide d) shallower junction

(vii) Identify that short channel effect can be characterized by
   a) saturation drain current depends quadratically upon overdrive voltage b) bulk depletion region becomes assymetrical in shape instead of a rectangular structure
   c) drain depletion region becomes larger than source depletion region d) threshold voltage decreases with effective channel length

(viii) Identify how many carbon atom present in C80 Fullerene

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a) 40 b) 60
c) 120 d) 80

(ix) Identify which one have faster switching speed
a) Double gate MOSFET b) FinFET
c) Surrounding gate MOSFET d) none of these

(x) For the synthesis of CNTs, choose the maximum temperature for which the quartz tube is heated up
a) 1000°C b) 1200°C
c) 1400°C d) 1600°C

(xi) Choose the correct application of CNT from the following
a) Paper batteries b) High voltage batteries
c) Car batteries d) Clock batteries

(xii) Identify the carbon nanostructure with which CNTs are capped on both ends
a) Graphite b) Diamond
c) C60 d) Benzene

(xiii) Choose the significant advantage of Single Electron Transistors
a) High-speed operation b) Low power consumption
c) Large size d) High fabrication complexity

(xiv) Indicate that an SET differ from a conventional transistor because
a) SETs have higher power consumption b) SETs operate at room temperature
c) SETs control single electrons d) SETs have lower fabrication costs

(xv) For the operation of enhancement only N-channel MOSFET , identify the nature of gate voltage
a) Positive b) Negative
c) Zero d) none of these

Group-B

(Short Answer Type Questions) 3 x 5=15

2. State and explain Moore's Law. (3)

3. Discuss the advantage of double gate MOSFET. (3)

4. Explain the various applications of quantum dots. (3)

5. Describe Eigen value and Eigen function. (3)

6. Distinguish diamond and graphite. (3)

OR

Distinguish single wall nanotube and multiwall nanotube. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain why gate-engineering techniques are used for reduction of SCEs. (5)

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8. Explain the potential applications of resonant tunnelling diode. (5)

9. Justify the density of state is dependent on the dimension of a material by the following relation (5)

$$D(E) \propto E^{\frac{d}{2}-1}$$

Where d is thee dimensionality of the system.

10. Describe Short Channel Effects. (5)

11. Describe the nanoscale MOSFET and its advantages in semiconductor technology. (5)

12. Compare different types of hybridization observed in carbon. (5)

OR

Compare Single Electron Transistor and Conventional Transistor. (5)

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