BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Diploma in Computer Science & Engineering

Course Name – Computer Organization

Course Code - DCSE301

Semester / Year - Semester III

Time allotted : 85 Minutes Full Marks : 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 70=70

1. *(Answer any Seventy)*

(i) Which of the following is a universal logic gate?

a) XOR b) NOR

c) OR d) XNOR

(ii) The format which is usually used to store data is

a) Decimal b) Octal

c) Binary d) Hexadecimal

(iii) If the searched data is found in the desired memory, it is said to be

a) hit ratio b) miss

c) hit d) hit rate

(iv) Von Neumann architecture is based on

a) stored data concept b) stored program concept

c) stored instruction concept d) stored signal concept

(v) Which of the following is not a bus

a) control bus b) data bus

c) program bus d) address bus

(vi) Maximum n bit 2 s complement number is

a) 2n
b) 2n -1
c) 2n-1 - 1
d) cannot said

(vii) Booth's algorithm is used for performing binary

a) addition
b) multiplication
c) division
d) subtraction

(viii) The 2s compliment form (Use 6 bit word) of the number 1010 is

a) 111100
b) 110110
c) 110111
d) 1011

(ix) Which of the following is used to hold the data that is being transferred to or from memory

a) Accumulator
b) MAR
c) Program Counter
d) MDR

(x) Which of the following is an exclusive form of OR logic gate?

a) NOR
b) XNOR
c) OR
d) XOR

(xi) In which cycle the memory is read and the contents of memory at the address contained in the PC register are loaded into Instruction Register

a) Execution Cycle
b) Memory Cycle
c) Decode Cycle
d) Fetch Cycle

(xii) Every instruction cycle consists of

a) Fetch Cycle
b) Execute Cycle
c) Both Fetch Cycle and Execute cycle
d) only Exeute Cycle

(xiii) The time required to complete one instruction is called

a) Fetch time
b) Execution time
c) Control time
d) All of these

(xiv) Operation of memory transfer is/are

a) Read
b) Write
c) Both Read and Write
d) None

(xv) How many bits are needed to represent a digit in hexadecimal notation?

a) 8
b) 16
c) 4
d) 2

(xvi) Over flow occurs when

a) data is out of range
b) data is within range
c) Both data is out of range and Data is within range
d) none of these

(xvii) Main difference between CISC and RISC

a) RISC has few registers
b) RISC has few addressing modes
c) CISC has more registers
d) All of these

(xviii) The step during which the operations specified by the instruction are processed

a) decode
b) fetch
c) execute
d) none of these

(xix) Periodic refreshing is needed in

a) ROM
b) EPROM
c) SRAM
d) DRAM

(xx) Sub tractor can be implemented using

a) adder
b) complementer

c) Both adder and complementer
d) none of these

(xxi) DMA stands for

a) Discrete memory architecture
b) Discrete memory access
c) Direct memory architecture
d) Direct memory access

(xxii) The algorithm to remove and place new contents into the cache is called

a) Renewal algorithm
b) Replacement algorithm
c) Mapping algorithm
d) None

(xxiii) Which of the following is used to store intermediate result

a) Accumulator
b) MAR
c) MDR
d) Program Counter

(xxiv) The method which offers higher speeds of I/O transfers is

a) interrupts
b) memory mapping
c) program controlled I/O
d) direct memory access

(xxv) Size of the _____ memory mainly depends on the size of the address bus.

a) Main
b) Virtual
c) Secondary
d) Cache

(xxvi) Which of the following has smallest capacity

a) cache memory
b) RAM
c) secondary memory
d) registers

(xxvii) Write Through technique is used in which memory for updating the data

a) Virtual memory
b) Cache memory
c) Main memory
d) Auxiliary memory

(xxviii) Virtual memory consists of

a) SRAM
b) DRAM
c) Magnetic memory
d) None of these

(xxix) Cache memory works on the principle of

a) Locality of reference
b) Locality of memory
c) Locality of data
d) Locality of data and memory

(xxx) A Single bus structure is primarily found in

a) mini and micro computers
b) large mainframe computers
c) super computer
d) analog computers

(xxxi) Instruction pipeline can be implemented by means of

a) LIFO buffer
b) Stack
c) FIFO buffer
d) None of above

(xxxii) An address in main memory is called

a) Physical address
b) Logical address
c) Memory address
d) Word address

(xxxiii) An interface that provides I/O transfer of data directly to and from the memory unit and peripheral is termed as

a) DDA
b) Serial interface
c) BR
d) DMA

(xxxiv) A register capable of shifting its binary information either to the right or the left is called a

a) parallel register
b) serial register
c) shift register
d) storage register

(xxxv) In which addressing mode the operand is given explicitly in the

instruction

a) Absolute
b) Immediate
c) Indirect
d) Direct

(xxxvi) Program always deals with

a) logical address
b) absolute address
c) physical address
d) relative address

(xxxvii) Memory management technique in which system stores and retrieves data from secondary storage for use in main memory is called

a) fragmentation
b) paging
c) mapping
d) none of above

(xxxviii) A memory used to store frequent used data

a) stack pointer
b) accumulator
c) cache
d) disk buffer

(xxxix) Cache memory-

a) has greater capacity than RAM
b) is faster to access than CPU Registers
c) is permanent storage
d) faster to access than RAM

(xl) Which memory unit has lowest access time?

a) cache
b) registers
c) main memory
d) magnetic disk

(xli) Virtual memory is –

a) an extremely large main memory
b) an extremely large secondary memory
c) an illusion of an extremely large memory
d) None of these

(xlii) The user view of memory is supported by

a) paging
b) segmentation

c) both
d) none

(xliii) Data hazards occur when

a) Greater performance loss
b) Machine size is limited
c) Some functional unit is not fully pipelined
d) Pipeline changes the order of read/write access to operands

(xliv) The difference circuit in full sub tractor is implemented using

a) XOR
b) OR
c) AND
d) NOT

(xlv) Pipeline implement

a) Fetch instruction
b) Execute instruction
c) Decode instruction
d) All of these

(xlvi) The average time required to reach a storage location in memory and obtain its contents is called

a) Latency time
b) Access time
c) Turnaround time
d) Response time

(xlvii) RISC stands for cache memory is used to

a) Remodeled Interface System Computer
b) Remote Intranet Secured Connection
c) Reduced Instruction Set Computer.
d) Runtime Instruction Set Compiler

(xlviii) Hardware devices that are not part of the main computer system and are often added later to the system

a) Peripheral
b) Clip art
c) Highlight
d) None of these

(xlix) MAR stands for _____

a) Memory Address register
b) Main Address register

c) Main accessible register
d) Memory accessible register

(l) If M denotes the number of memory locations and N denotes the word size, then an expression that denotes the storage capacity is _____.

a) M*N
b) M+N
c) 2M+N
d) 2M-N

(li) Which of the following is the fastest means of memory access for CPU?

a) Register
b) Cache
c) Main Memory
d) Virtual memory

(lii) The two phases of executing an instruction are _____

a) Instruction decoding and storage
b) Instruction fetch and instruction execution
c) Instruction execution and storage
d) Instruction fetch and Instruction processing

(liii) The Instruction fetch phase ends with _____

a) Placing the data from the address in MAR into MDR
b) Placing the address of the data into MAR
c) Completing the execution of the data and placing its storage address into MAR
d) Decoding the data in MDR and placing it in IR

(liv) BCD uses binary number system to specify decimal numbers

a) 1.0-10
b) 1.0-9
c) 0-9
d) 0-10

(lv) BR signal in DMA stands for

a) bus record
b) bus register
c) bus request
d) buffer register

(lvi) The signal sent by the CPU to the DMA controller to take control over buses

a) BG
b) ACK
c) BR
d) DMA

(lvii) The secondary storage memory is also called

a) main memory
b) auxiliary memory
c) shared memory
d) all of these

(lviii) Interrupts which are initiated by an I/O drive are

a) internal
b) external
c) software
d) all of above

(lix) _____ is generally used to increase the apparent size of physical memory.

a) Secondary memory
b) Virtual memory
c) Hard Disk
d) Disk

(lx) The addressing mode, where you directly specify the operand value is _____

a) Immediate
b) Direct
c) Define
d) Relative

(lxi) SIMD stands for

a) Single instruction memory data
b) Single information multiple data
c) Sequence information multiple data
d) Single instruction multiple data

(lxii) Pipelining strategy is called implement

a) instruction execution
b) instruction prefetch
c) instruction execution
d) instruction manipulation

(lxiii) A stack pointer is

a) a 16-bit register in the microprocessor that indicate the beginning of the stack memory

b) a register that decodes and executes 16-bit arithmetic expression.

c) The first memory location where a subroutine address is stored.

d) a register in which flag bits are stored

(lxiv) Which of the register/s of the processor is/are connected to Memory Bus?

a) PC

b) MAR

c) IR

d) Both PC and MAR

(lxv) The average time required to access a data its given memory locations

a) seek time

b) access time

c) turnaround time

d) transfer time

(lxvi) The 8-bit encoding format used to store data in a computer is _____

a) ASCII

b) EBCDIC

c) ANCI

d) USCII

(lxvii) DRAM is used as main memory as it

a) consumes less power

b) has high speed

c) has lower cell density

d) needs refreshing circuitry

(lxviii) The control unit controls other units by generating _____

a) Control Signals

b) Timing Signals

c) Transfer Signals

d) Command Signals

(lxix) Booth's Algorithm is applied on _____

a) decimal numbers

b) binary numbers

c) hexadecimal numbers

d) octal Numbers

(lxx)

Which of the following is an universal logic gate?

a)

AND(N)

b) NAND(Y)

c) OR(N)

d) XOR(N)