BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Diploma in Computer Science & Engineering

Course Name – Digital Electronics

Course Code - DCSE303

Semester / Year - Semester III

Time allotted : 75 Minutes Full Marks : 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 60=60

1. *(Answer any Sixty)*

(i)

Binary subtraction of 100101 – 011110 is

a) 000111 b) 010101

c) 111000 d) 101010

(ii)

On subtracting $(001100)_2$ from $(101001)_2$ using 2's complement, we get

a) 1101100 b) 11101

c) 11010101 d) 11010111

(iii) The digit F in Hexadecimal system is equivalent to …… in decimal system.

a) 13 b) 14

c) 15 d) 17

(iv) Solution of(11001)2 – (10001)2 is

a) 10000 b) 1000

c) 100 d) 1

(v) The digit 10001 in Binary system is equivalent to …… in Hexadecimal

system

a) 10 b) 11

c) D d) F

(vi) Which is the prohibited state/ condition in S-R latch and needs to be avoided due to unpredictable nature of output?

a) S = R = 0 b) S = 0, R = 1

c) S = 1, R = 0 d) S = R = 1

(vii) In the toggle mode a JK flip-flop has

a) J = 0, K = 0 b) J = 1, K = 1

c) J = 0, K = 1 d) J = 1, K = 0

(viii)

The decimal equivalent of the binary number $(1011.011)_2$ is

a) b)

$(11.375)_{10}$ $(10.123)_{10}$

c) d)

$(11.175)_{10}$ $(9.23)_{10}$

(ix) The decimal number 10 is represented in its BCD form as

a) 10100000 b) 1010111

c) 10000 d) 101011

(x)

The octal equivalent of the decimal number $(417)_{10}$ is

a) b)

$(641)_8$ $(619)_8$

c) d)

$(640)_8$ $(598)_8$

(xi) In Boolean algebra, the OR operation is performed by which properties

a) Associative properties b) Commutative properties

c) Distributive properties d) All of these

(xii) The boolean function A + BC is a reduced form of

a) AB + BC b) (A + B)(A + C)

c) A'B + AB'C d) (A + C)B

(xiii) The expression Y=(A+B)(B+C)(C+A) shows the _____ operation.

a) AND b) NAND

c) SOP d) POS

(xiv) The canonical sum of product form of the function y(A,B) = A + B is

a) AB + BB + A'A b) AB + AB' + A'B

c) BA + BA' + A'B' d) AB' + A'B + A'B'

(xv) There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and _____ operations.

a) X-NOR b) X-OR

c) NOR d) NAND

(xvi) How many AND & OR gates are required to realize Y = CD + EF + G?

a) 4 b) 5

c) 2 d) 3

(xvii) The NOR gate output will be high if the two inputs are

a) 0 b) 1

c) 10 d) 11

(xviii) The gates required to build a half adder are

a) EX-OR gate and NOR gate b) EX-OR gate and OR gate

c) EX-OR gate and AND gate d) EX-OR gate and NAND gate

(xix) A digital system consists of _____ types of circuits.

a) 2 b) 3

c) 4 d) 5

(xx) In a sequential circuit, the output at any time depends only on the input values at that time.

a) Past output values b) Intermediate values

c) Both past output and present input d) Present input values

(xxi) In which operation carry is obtained?

a) Subtraction b) Addition

c) Multiplication d) Both addition and subtraction

(xxii) Half subtractor is used to perform subtraction of

a) 2 bits b) 3 bits

c) 4 bits d) 5 bits

(xxiii) The output of a subtractor is given by (if A, B and X are the inputs)

a) A AND B XOR X b) A XOR B XOR X

c) A OR B NOR X d) A NOR B XOR X

(xxiv) The output of a full subtractor is same as

a) Half adder b) Full adder

c) Half subtractor d) Decoder

(xxv) When performing subtraction by addition in the 2's-complement system

a) The minuend and the subtrahend are both changed to the 2's-complement

b) The minuend is changed to 2's-complement and the subtrahend is left in its original form

c) The minuend is left in its original form and the subtrahend is changed to its 2's-complement

d) The minuend and subtrahend are both left in their original form

(xxvi) TTL is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by

a) Resistors

b) Bipolar junction transistors

c) One transistor

d) Resistors and transistors respectively

(xxvii) Standard TTL circuits operate with a __ volt power supply

a) 2

b) 5

c) 4

d) 6

(xxviii) In RTL NOR gate, the output is at logic 1 only when all the inputs are at

a) logic 0

b) logic 1

c) +10V

d) Floating

(xxix) The role of the _____ is to convert the collector current into a voltage in RTL.

a) Collector resistor

b) Base resistor

c) Capacitor

d) Inductor

(xxx) The primary advantage of RTL technology was that

a) It results as low power dissipation

b) It uses a minimum number of resistors

c) It uses a minimum number of transistors

d) It operates swiftly

(xxxi) TTL circuits with "totem-pole" output stage minimize

a) The power dissipation in RTL
b) The time consumption in RTL
c) The speed of transferring rate in RTL
d) Propagation delay in RTL

(xxxii) How many stages a DTL consist of?

a) 2
b) 3
c) 4
d) 5

(xxxiii) The full form of ECL is

a) Emitter-collector logic
b) Emitter-complementary logic
c) Emitter-coupled logic
d) Emitter-cored logic

(xxxiv) In an ECL the output is taken from

a) Emitter
b) Base
c) Collector
d) Junction of emitter and base

(xxxv) The ECL circuits usually operates with

a) Negative voltage
b) Positive voltage
c) Grounded voltage
d) High Voltage

(xxxvi) How many shift registers are used in a 4 bit serial adder?

a) 2
b) 3
c) 4
d) 5

(xxxvii) Which of the following circuit can be used as parallel to serial converter?

a) Multiplexer
b) De-multiplexer
c) Decoder
d) Digital counter

(xxxviii) A digital multiplexer is a Combinational circuit that selects

a) One digital information from several sources and transmits the selected one
b) Many digital information and convert them into one

c) Many decimal inputs and transmits the selected information

d) Many decimal outputs and accepts the selected information

(xxxix) How many NOT gates are required for the construction of a 4-to-1 multiplexer?

a) 3

b) 4

c) 2

d) 5

(xl) One multiplexer can take the place of

a) Several SSI logic gates

b) Combinational logic circuits

c) Several Ex-NOR gates

d) Several SSI logic gates or combinational logic circuits

(xli) Most de-multiplexers facilitate which type of conversion?

a) Decimal-to-hexadecimal

b) Single input, multiple outputs

c) AC to DC

d) Odd parity to even parity

(xlii) The odd parity output of decimal number 9 is

a) 0

b) 1

c) 11

d) 1001

(xliii) (1D)16 in BCD 8421 code is

a) 11101

b) 101001

c) 11101

d) 1100011

(xliv) For a code to be self-complementing the sum of all its weighs must be

a) 6

b) 9

c) 10

d) 12

(xlv) 8421 code is

a) self - complementing code

b) weighted code

c) non-weighted code
d) alphanumeric code

(xlvi) Which of the following codes is known as the 8421 code?

a) Gray code
b) XS-3 code
c) ASCII code
d) BCD code

(xlvii) An X-OR gate gives a high output

a) if there are odd number of 1s
b) if it has even number of 0s
c) if the decimal value of digital word is even
d) for odd decimal value

(xlviii) The output of a logic gate is 0 when all its input are a logic 1 the gate is either

a) an NAND or an AND
b) an NAND or an XOR
c) an NOR or an XNOR
d) an NAND or a XNOR

(xlix) A +A' B + A'B'C + A'B'C' D +.... =

a) A + B + C+....
b) A' + B' + C'+ D' +....
c) 1
d) 0

(l) A +B=B+A; AB=BA represents which laws?

a) commutative
b) associative
c) distributive
d) idempotence

(li) How many inputs and outputs does a full-adder have ?

a) two inputs , two outputs
b) two inputs , one output
c) three inputs , two outputs
d) two inputs , three outputs

(lii) Parallel adders are

a) combinational logic circuits
b) sequential logic circuits
c) both of these
d) none of these

(liii) BCD subtractions is performed by using

a) 1's complement representation
b) 2's complement representation
c) 5's complement representation
d) 9's complement representation

(liv) A logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output is called

a) a multiplexer
b) a demultiplexer
c) a transmitter
d) a receiver

(lv) A multiplexer with four select bits is a

a) 4:1 multiplexer
b) 8:1 multiplexer
c) 16:1 multiplexer
d) 32:1 multiplexer

(lvi) A MUX with its address bits generated by a counter operates as a

a) parallel-to-serial converter
b) serial-to-parallel converter
c) modified counter
d) modified multiplexer

(lvii) A flip-flop has two outputs which are

a) always 0
b) always 1
c) always complementary
d) All of these

(lviii) The race around condition occurs in a J-K flip-flop when

a) both inputs are 0
b) both inputs are 1
c) the inputs are complementary
d) any one of the above input combinations is present

(lix) Master slave configuration is used in flip-flops to

a) increase its clocking rate
b) reduce power dissipation
c) eliminate race-round condition
d) improve its reliability

(lx) The output Qn of a J-K flip-flop is 1. it changes to 0 when a clock pulse is

applied. the input Jn and Kn are respectively

a) 0 and X

b) `1 and X

c) X and 1

d) X and 0