BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Diploma in Electronics & Communication Engineering

Course Name – Digital Electronics

Course Code - DECE303

Semester / Year - Semester III

Time allotted : 75 Minutes Full Marks : 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 60=60

1. *(Answer any Sixty)*

(i) Convert binary number into gray code: 100101

a) 101101 b) 001110

c) 110111 d) 111001

(ii) A binary-to-octal decoder is a

a) 3-line to 8-line decoder b) 1-line to 8-line decoder

c) 4-line to 8-line decoder d) none of these

(iii) A multiplexer is also known as a data _____.

a) accumulator b) restorer

c) selector d) distributor

(iv) A flip-flop can store

a) one bit of data b) two bits of data

c) three bits of data d) any number of bits of data

(v) Flip-flops can be used to make _____.

a) latches b) bounce –elimination switches

c) registers d) all of these

(vi) How many states a 6-bit ripple counter can have?

a) 6 b) 16

c) 32 d) 64

(vii) The minimum number of 4-to-1 multiplexers required to realize a 16-to-1 multiplexer is _____.

a) 4 b) 5

c) 6 d) 8

(viii) A device which can convert binary to octal is

a) Encoder b) Multiplexer

c) Demultiplexer d) Decoder

(ix) The expression Y=(A+B)(B+C)(C+A) shows-

a) AND operation b) POS operation

c) SOP operation d) NAND operation

(x)

Binary subtraction of 100101 – 011110 is_____.

a) 000111 b) 111000

c) 010101 d) 101010

(xi) Which of the following is the fastest logic?

a) ECL b) TTL

c) CMOS d) LSI

(xii) Why is a demultiplexer called a data distributor?

a) The input will be distributed to one of the outputs b) One of the inputs will be selected for the output

c) The output will be distributed to one of d) Single input gives single output

the inputs

(xiii) Most demultiplexers facilitate which type of conversion?

a) Decimal-to-hexadecimal
b) Single input, multiple outputs
c) AC to DC
d) Odd parity to even parity

(xiv) In 1-to-4 demultiplexer, if the two select line C1 = 1 & C2 = 1, then the output will be _____

a) Y0
b) Y1
c) Y2
d) Y3

(xv) The number of control lines for 32 to 1 multiplexer is

a) 4
b) 5
c) 16
d) 6

(xvi)

The binary equivalent of $(FA)_{16}$ is

a) 1010 1111
b) 1111 1010
c) 10110011
d) none of these

(xvii) Convert decimal 153 to octal. Equivalent in octal will be

a)
b)

$(231)_8$
$(331)_8$

c)
d) none of these

$(431)_8$

(xviii) Which of following requires refreshing?

a) SRAM
b) DRAM
c) ROM
d) EPROM

(xix) How many address bits are required to represent a 32 K memory?

a) 10 bits
b) 12 bits
c) 14 bits
d) 15 bits

(xx) The 2's complement of the number 1101110 is

a) 10001
b) 10001
c) 10010
d) None of these

(xxi) An eight stage ripple counter uses a flip-flop with propagation delay of 75 nanoseconds. The pulse width of the strobe is 50ns. The frequency of the input signal which can be used for proper operation of the counter is approximately

a) 1 MHz
b) 500 MHz
c) 2 MHz
d) 4 MHz

(xxii) A full adder logic circuit will have

a) Two inputs and one output
b) Three inputs and three outputs
c) Two inputs and two outputs
d) Three inputs and two outputs

(xxiii) The excess-3 code of decimal 7 is represented by

a) 1100
b) 1001
c) 1011
d) 1010

(xxiv) How many flip-flops are required to construct mod 30 counter

a) 5
b) 6
c) 4
d) 8

(xxv) Which of following are known as universal gates?

a) NAND & NOR
b) AND & OR
c) XOR & XNOR
d) None of these

(xxvi) How many address bits are required to represent 4K memory?

a) 5 bits
b) 12 bits
c) 8 bits
d) 10 bits

(xxvii) How many AND gates are required to realize Y = CD+EF+G

a) 4
b) 5
c) 3
d) 2

(xxviii) In a positive logic system, logic state 1 corresponds to

a) positive voltage
b) higher voltage level
c) zero voltage level
d) lower voltage level

(xxix) The process of entering data into a ROM is called _____.

a) burning in the ROM
b) programming the ROM
c) changing the ROM
d) charging the ROM

(xxx) The device which changes from serial data to parallel data is

a) counter
b) multiplexer
c) demultiplexer
d) flip-flop

(xxxi) When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?

a) Sign-magnitude
b) 1's complement
c) 2's complement
d) 9's complement

(xxxii) The decimal equivalent of Binary number 11010 is_____.

a) 26
b) 36
c) 16
d) 23

(xxxiii) The excess 3 code of decimal number 26 is_____.

a) 0100 1001
b) 0101 1001

c) 1000 1001 d) 0100 1101

(xxxiv) A ring counter consisting of five Flip-Flops will have _____.

a) 5 states b) 10 states

c) 32 states d) Infinite states.

(xxxv) When simplified with Boolean Algebra, (x + y)(x + z) simplifies to

a) x b) x + x(y + z)

c) x(1 + yz) d) x + yz

(xxxvi) De Morgan's first theorem shows the equivalence of -

a) OR gate and XOR gate b) NOR gate and Bubbled AND gate

c) NOR gate and NAND gate d) NAND gate and NOT gate

(xxxvii) EPROM contents can be erased by exposing it to

a) Ultraviolet rays b) Infrared rays

c) Burst of microwaves d) Intense heat radiations

(xxxviii) The output of a logic gate is 1 when all its inputs are at logic 0. the gate is either

a) a NAND or an EX-OR b) an OR or an EX-NOR

c) an AND or an EX-OR d) a NOR or an EX-NOR

(xxxix) 1's complement can be easily obtained by using

a) Comparator b) Inverter

c) Adder d) Subtractor

(xl) What is the octal equivalent of the binary number: 10111101

a) 675 b) 275

c) 572 d) 573

(xli)

Convert $(0.345)_{10}$ into an octal number

a) $(0.16050)_8$

b) $(0.26050)_8$

c) $(0.19450)_8$

d) $(0.24040)_8$

(xlii) The inverter can be produced with how many NAND gates?

a) 1

b) 2

c) 3

d) 4

(xliii)

The decimal equivalent of the binary number $(1011.011)_2$ is

a) $(11.375)_{10}$

b) $(10.123)_{10}$

c) $(11.175)_{10}$

d) $(9.23)_{10}$

(xliv) The output of a logic gate is 0 when all its input are a logic 1 the gate is either

a) an NAND or an AND

b) an NAND or an XOR

c) an NOR or an XNOR

d) an NAND or a XNOR

(xlv) The simplified form of the Boolean expression (X+Y+XY)(X+Z) is

a) X+Y+Z

b) XY+YZ

c) X +YZ

d) XZ+Y

(xlvi) A multiplexer with four select bits is a

a) 4:1 multiplexer
b) 8:1 multiplexer
c) 16:1 multiplexer
d) 32:1 multiplexer

(xlvii) A 4-variable logic circuit can be designed using

a) a 16:1 multiplexer
b) an 8:1 multiplexer and one inverter
c) two 8:1 multiplexers and one 2:1 multiplexer
d) any of these

(xlviii) A full-adder can be realized using

a) one half-adder, two OR gates
b) two half-adder, one OR gates
c) two half-adders, two OR gates
d) two half-adders, one AND gates

(xlix) The of 4-line to -16 line decoders required to make an 8-line to 256-line decoder is

a) 16
b) 17
c) 32
d) 64

(l) In general, a sequential logic circuit consists of

a) only flip-flops
b) only gates
c) flip-flops and combinational logic circuits
d) only combinational logic circuits

(li) When a flip-flop is set , its outputs will be

a) Q=0 , Q' = 0
b) Q=1 , Q' = 0
c) Q=0 , Q' = 1
d) Q=1 , Q' = 1

(lii) A shift register using flip-flop is called a

a) dynamic shift register
b) flip-flop shift register
c) static shift register
d) buffer shift register

(liii) The characteristic equation of a J-K flip-flop is

a) Q n+1= JQn' + K'Qn
b) JQn' + K'Qn
c) J'Qn + K'Qn
d) J'Q'n + KQn

(liv) The characteristic equation of a T flip-flop is

a) Q n+1= Qn'T + Qn T'
b) Q n+1= Qn'T' + Qn T
c) Q n+1= Qn
d) Q n+1= Q'n

(lv) TTL is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by

a) Resistors
b) Bipolar junction transistors
c) One transistor
d) Resistors and transistors respectively

(lvi) TTL is a

a) Current sinking
b) Current sourcing
c) Voltage sinking
d) Voltage sourcing

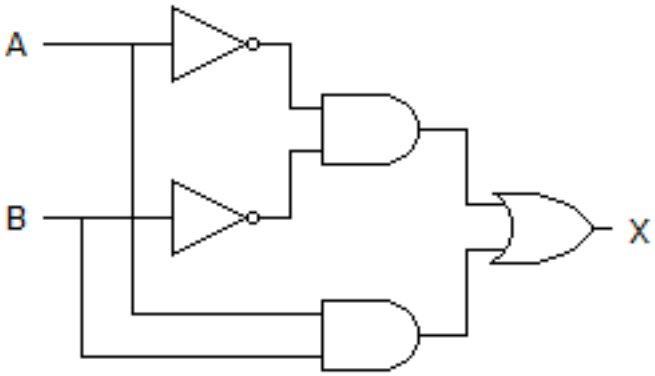
(lvii)

$(A+B)(\overline{A+B})$ =

a)
b) 0
1
c) AB
d) $A\overline{B}$

(lviii)

Which of the following logic expressions represents the logic diagram shown in figure?



a)

X=AB'+A'B

b)

X=(AB)'+AB

c)

X=(AB)'+A'B'

d)

X=A'B'+AB

(lix)

Before an SOP implementation, the expression $X = AB(\overline{C}D + EF)$ would require a total of how many gates?

a) 1
b) 2
c) 4
d) 5

(lx)

How many AND gates are required to implement the Boolean expression, $X = AB\overline{C} + A\overline{B}C + \overline{A}BC$?

a) 1
b) 2
c) 3
d) 4