BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Bachelor of Technology in Computer Science & Engineering

Course Name – Digital Electronics

Course Code - ESC(CSE)302

Semester / Year - Semester III

Time allotted : 75 Minutes | Full Marks : 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 60=60

1. *(Answer any Sixty)*

(i) Karnaugh map is used:

a) To draw the digital circuit layout
b) To simplify logical function
c) To locate different gates in a digital circuit
d) None of these

(ii) How many AND gates are required for a 8-to-1 multiplexer?

a) 5
b) 7
c) 8
d) 6

(iii) Full subtractor is used to perform subtraction of _____.

a) 4 bits
b) 3 bits
c) 2 bits
d) 8 bits

(iv) Which is the prohibited state/ condition in S-R latch and needs to be avoided due to unpredictable nature of output?

a) S = R = 0
b) S = 0, R = 1
c) S = 1, R = 0
d) S = R = 1

(v)

In 1:4 demultiplexer, if $S_0 = 1$ & $S_1 = 1$, then the output will be _____.

a) Y_0

b) Y_1

c) Y_2

d) Y_3

(vi) The largest two digit hexadecimal number is _____.

a) $(FE)_{16}$

b) $(FD)_{16}$

c) $(FF)_{16}$

d) $(EF)_{16}$

(vii) The expression Y=(A+B)(B+C)(C+A) shows the _____ operation.

a) AND

b) POS

c) SOP

d) NAND

(viii) How many AND & OR gates are required to realize Y = CD + EF + G?

a) 4

b) 5

c) 3

d) 2

(ix) A full adder logic circuit will have _____.

a) Two inputs and one output

b) Three inputs and three outputs

c) Two inputs and two outputs

d) Three inputs and two outputs

(x) The gates required to build a half adder are _____.

a) EX-OR gate and NOR gate

b) EX-OR gate and OR gate

c) EX-OR gate and AND gate

d) EX-NOR gate and AND gate

(xi) Exclusive-OR (XOR) logic gates can be constructed from what other logic