BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Master of Science in Computer Science

Course Name – Advanced Computer Architecture

Course Code - MCS301

Semester / Year - Semester III

Time allotted : 75 Minutes | Full Marks : 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 60=60

1. *(Answer any Sixty)*

(i) Which of the following is a universal logic gate?

a) XOR b) NOR

c) OR d) XNOR

(ii) If the searched data is found in the desired memory, it is said to be

a) Hit ratio b) Miss

c) Hit d) Hit rate

(iii) Which of the following is not a bus?

a) Control bus b) Data bus

c) Program bus d) Address bus

(iv) The RISC processor design is more _____ than CISC

a) Simpler b) Complicated

c) Smaller d) None of these

(v) Both the CISC and RISC architectures have been developed to reduce the _____

a) Cost b) Time delay

c) Semantic gap d) All of these

(vi) Which is not a data hazard?

a) WAR
b) RAW
c) RAR
d) WAW

(vii) The method which offers higher speeds of I/O transfers is

a) Interrupts driven
b) Memory mapping
c) Program controlled I/O
d) Direct memory access

(viii) Which of the following is used to store the address of next instruction?

a) Accumulator
b) MAR
c) Program Counter
d) MDR

(ix) Booth's algorithm is used for performing binary

a) addition
b) multiplication
c) division
d) subtraction

(x) Which is a part of Flynn's classification?

a) MIMD
b) SISD
c) MISD
d) All of these

(xi) Software in computer

a) Enhances the capabilities of the hardware machine
b) Increase the speed of central processing unit
c) Both of these
d) None of these

(xii) People often call _____ as the brain of computer system

a) Control Unit
b) Arithmetic Logic Unit
c) Central Processing Unit
d) Storage Unit

(xiii) BCD is

a) Binary Coded Decimal
b) Bit Coded Decimal

c) Binary Coded Digit
d) Bit Coded Digit

(xiv) Which is the main part of Central Processing Unit (CPU)?

a) ALU
b) CU
c) Memory unit
d) Input/output unit

(xv) Which of the following is true about RAM (Random access memory)?

a) It is used as read/write memory
b) It is non-volatile memory
c) It is possible to retrieve information randomly
d) It retains information as long as power supply is on

(xvi) The computer architecture aimed at reducing the time of execution of instructions is _____

a) CISC
b) RISC
c) ISA
d) ANNA

(xvii) In half subtractor, the difference circuit is implemented using

a) XOR
b) AND
c) OR
d) NOT

(xviii) Floating point representation is used to store

a) Boolean values
b) Whole numbers
c) Real integers
d) Integers

(xix) The average time required to access a data its given memory locations

a) seek time
b) access time
c) turnaround time
d) transfer time

(xx) Von Neumann architecture is

a) SISD
b) SIMD
c) MISD
d) MIMD

(xxi) Virtual memory consists of

a) SRAM
b) DRAM
c) Magnetic memory
d) None of these

(xxii) Cache memory works on the principle of

a) Locality of reference
b) Locality of memory
c) Locality of data
d) Locality of data and memory

(xxiii) Memory unit accessed by content is called

a) ROM
b) Virtual memory
c) Programmable memory
d) Associative memory

(xxiv) Write Through technique is used in which memory for updating the data

a) Virtual memory
b) Main memory
c) Cache memory
d) Auxiliary memory

(xxv) Instruction pipeline can be implemented by means of

a) LIFO buffer
b) Stack
c) FIFO buffer
d) None of these

(xxvi) An address in main memory is called

a) Physical address
b) Logical address
c) Memory address
d) Word address

(xxvii) Which of the following is not an example of primary memory?

a) RAM
b) ROM
c) Cache memory
d) Magnetic tape

(xxviii) A register capable of shifting its binary information either to the right or the left is called a

a) parallel register
b) serial register

c) shift register
d) storage register

(xxix) SISD stands for

a) Single instruction single data
b) Single information single data
c) Sequence instruction single data
d) Single instruction sequence data

(xxx) Program always deals with

a) logical address
b) absolute address
c) physical address
d) relative address

(xxxi) A memory used to store frequent used data

a) stack pointer
b) accumulator
c) cache
d) disk buffer

(xxxii) CPU fetches the instruction from memory according to the value of

a) program counter
b) instruction register
c) status register
d) program status word

(xxxiii) The addressing mode, where the operand value is implicitly specified

a) implied
b) direct
c) immediate
d) indirect

(xxxiv) Which is/are data hazard

a) WAR
b) RAW
c) WAW
d) All of these

(xxxv) Pipeline implement

a) Fetch instruction
b) Execute instruction
c) Decode instruction
d) All of these

(xxxvi) The total number of possible combinations if number of inputs are n

a) 2n
b) nn
c) n2
d) None of these

(xxxvii) In which cycle the memory is read and the contents of memory at the address contained in the PC register are loaded into Instruction Register

a) Execution Cycle
b) Memory Cycle
c) Decode Cycle
d) Fetch Cycle

(xxxviii) Two important fields of an instruction are

a) Opcode
b) Operand
c) Only Opcode
d) Both Opcode & Operand

(xxxix) The sequence of operations performed by CPU in processing an instruction is

a) Execution cycle
b) Fetch cycle
c) Decode
d) Instruction cycle

(xl) The contention for the usage of a hardware device is called _____

a) Structural hazard
b) Stalk
c) Deadlock
d) None of these

(xli) VLIW stands for:

a) Vector Large Instruction Word
b) Very Long Instruction Word
c) Very Large Integrated Word
d) Very Low Integrated Word

(xlii) The algorithm to remove and place new contents into the cache is called _____

a) Replacement Algorithm
b) Renewal Algorithm
c) Updation
d) None of these

(xliii) The logical addresses generated by the CPU are mapped onto physical memory by ____

a) Relocation register
b) TLB
c) MMU
d) None of these

(xliv) The duration between the read and the MFC signal is _____

a) Access time
b) Latency
c) Delay
d) Cycle time

(xlv) The number of min terms for the function F(a, b, c, d, e) = b + cd is:

a) 24
b) 20
c) 32
d) 26

(xlvi) The write-through procedure is used _____

a) To write onto the memory directly
b) To write and read from memory simultaneously
c) To write directly on the memory and the cache simultaneously
d) None of these

(xlvii) The higher order bits of the address are used to _____

a) Specify the row address
b) Specify the column address
c) Input the CS
d) None of these

(xlviii) The address lines multiplexing is done using _____

a) MMU
b) Memory controller unit
c) Page table
d) Overlay generator

(xlix) The time taken to transfer a word of data to or from the memory is called as _____.

a) Access time.
b) Cycle time
c) Memory latency.
d) None of these

(l) Which is not a property of memory hierarchy?

a) Temporal
b) Spatial
c) Parallel
d) Sequential

(li) The difference between memory and storage is that the memory is____ and storage is_____

a) temporary, permanent
b) permanent, temporary
c) Slow, fast
d) None of these

(lii) A microprogram written as string of 0's and 1's is a

a) symbolic microinstruction
b) binary microinstruction
c) symbolic microprogram
d) binary microprogram

(liii) When a subroutine is called, the address of the instruction following the CALL instructions stored in/on the

a) stack pointer
b) accumulator
c) program counter
d) stack

(liv) Indicate which of the following is not true about an interpreter

a) Interpreter generates an object program from the entire source program
b) Interpreter is a kind of translator
c) Interpreter analyses each source statement every time it is to be executed
d) None of the above

(lv) Which of the following interrupt is non-maskable?

a) INTR
b) RST 6.5
c) TRAP
d) RST 7.5

(lvi) What is the content of Stack Pointer (SP)

a) Address of the current instruction
b) Address of the next instruction
c) Address of the top element of the stack
d) Size of the stack

(lvii) The main difference between a register and a counter is _____

a) A register has no specific sequence of states

b) A counter has no specific sequence of states

c) A register has capability to store one bit of information but counter has n-bit

d) A register counts data

(lviii) Registers capable of shifting in one direction is _____

a) Universal shift register

b) Unidirectional shift register

c) Unipolar shift register

d) Unique shift register

(lix) _____ is used to detect and correct the errors that may occur during data transfers

a) ECC

b) CRC

c) Checksum

d) None of these

(lx) The disk drive is connected to the system by using the _____

a) PCI bus

b) SCSI bus

c) HDMI

d) ISA