BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Bachelor of Technology in Electronics & Communication Engineering

Course Name – Digital System Design

Course Code - PCC-EC302

Semester / Year - Semester III

Time allotted : 85 Minutes Full Marks : 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 70=70

1. *(Answer any Seventy)*

(i) The decimal equivalent of hex number 1A53 is _____.

a) 6793 b) 6739

c) 6973 d) 6379

(ii) The number of select lines for a 8 – to – 1 multiplexer is_____.

a) 2 b) 3

c) 4 d) 5

(iii) EPROM contents can be erased by exposing it to?

a) Ultraviolet rays b) Infrared rays

c) Burst of microwaves d) Intense heat radiations

(iv) The output of a logic gate is 1 when all its inputs are at logic 0. the gate is either

a) a NAND or an EX-OR b) an OR or an EX-NOR

c) anAND or an EX-OR d) a NOR or an EX-NOR

(v) Data can be changed from special code to temporal code by using

a) shift registers b) counters

c) combinational circuits
d) A/D converters

(vi) When simplified with Boolean Algebra, (x + y)(x + z) simplifies to

a) x
b) x + x(y + z)
c) x(1 + yz)
d) x + yz

(vii) The gates required to build a half adder are

a) EX-OR gate and NOR gate
b) EX-OR gate and OR gate
c) EX-ORgate and AND gate
d) Four NAND gates.

(viii) The code where all successive numbers differ from their preceding number by single bit is

a) Binary code
b) BCD
c) Excess – 3
d) Gray

(ix) Which of the following is the fastest logic

a) TTL
b) ECL
c) CMOS
d) LSI

(x) If the input to T-flipflop is 100 Hz signal, the final output of the three T-flipflops in cascade is

a) 1000 Hz
b) 500 Hz
c) 333 Hz
d) 12.5 Hz

(xi) -8 is equal to signed binary number

a) 10001000
b) 1000
c) 10000000
d) 11000000

(xii) A device which converts BCD to Seven Segment is called

a) Encoder
b) Decoder
c) Multiplexer
d) Demultiplexer

(xiii) In a JK Flip-Flop, toggle means

a) Set Q = 1 and Q = 0
b) Set Q = 0 and Q = 1
c) Change the output to the opposite state
d) No change in output

(xiv) The access time of ROM using bipolar transistors is about

a) 1 sec
b) 1 msec
c) 1 μsec
d) 1 nsec.

(xv) A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be

a) 15 ns
b) 30 ns
c) 45 ns
d) 60 ns

(xvi) 1's complement representation of decimal number of -17 by using 8 bit representation is

a) 1110 1110
b) 1101 1101
c) 1100 1100
d) 0001 0001

(xvii) The excess 3 code of decimal number 26 is

a) 0100 1001
b) 01011001
c) 1000 1001
d) 1001101

(xviii) How many AND gates are required to realize Y = CD+EF+G

a) 4
b) 5
c) 3
d) 2

(xix) How many flip flops are required to construct a decade counter

a) 10
b) 3
c) 4
d) 2

(xx) In a RAM, information can be stored

a) By the user, number of times
b) By the user, only once
c) By the manufacturer, a number of times
d) By the manufacturer only once

(xxi) The MSI chip 7474 is

a) Dual edge triggered JK flip-flop (TTL)
b) Dual edge triggered D flip-flop (CMOS)
c) Dual edge triggered D flip-flop (TTL)
d) Dual edge triggered JK flip-flop (CMOS)

(xxii) The process of entering data into a ROM is called

a) burning in the ROM
b) programming the ROM
c) changing the ROM
d) charging the ROM

(xxiii) When the set of input data to an even parity generator is 0111, the output will be

a) 1
b) 0
c) Unpredictable
d) Depends on the previous input

(xxiv) The NOR gate output will be high if the two inputs are

a) 0
b) 1
c) 10
d) 11

(xxv) Which of following consume minimum power

a) TTL
b) CMOS
c) DTL
d) RTL

(xxvi) For JK flipflop J = 0, K=1, the output after clock pulse will be

a) 1
b) no change
c) 0
d) high impedance

(xxvii) How many address bits are required to represent 4K memory

a) 5 bits
b) 12 bits

c) 8 bits
d) 10 bits

(xxviii) How many select lines will a 32:1 multiplexer will have

a) 5
b) 8
c) 9
d) 11

(xxix) The decimal equivalent of Binary number 10101 is

a) 21
b) 31
c) 26
d) 28

(xxx) The output of a JK flipflop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the following conditions

a) By applying J = 0, K = 0 and using a clock
b) By applying J = 1, K = 0 and using the clock
c) By applying J = 1, K = 1 and using the clock
d) By applying a synchronous preset input

(xxxi) A full adder logic circuit will have

a) Two inputs and one output
b) Three inputs and three outputs
c) Two inputs and two outputs
d) Three inputs and two outputs

(xxxii) The logic 0 level of a CMOS logic device is approximately

a) 1.2 volts
b) 0.4 volts
c) 5 volts
d) 0 volts

(xxxiii) When an input signal A=11001 is applied to a NOT gate serially, its output signal is

a) 111
b) 110
c) 10101
d) 11001

(xxxiv) The number of flip flops contained in IC 7490 is

a) 2 b) 3

c) 4 d) 1

(xxxv) Shifting a register content to left by one bit position is equivalent to

a) division by two b) addition by two

c) multiplication by two d) subtraction by two

(xxxvi) The number of control lines for 256 to 1 multiplexer is

a) 5 b) 6

c) 3 d) 8

(xxxvii) Which of the following is the fastest logic?

a) ECL b) TTL

c) CMOS d) LSI

(xxxviii) Why is a demultiplexer called a data distributor?

a) The input will be distributed to one of the outputs b) One of the inputs will be selected for the output

c) The output will be distributed to one of the inputs d) Single input gives single output

(xxxix) In 1-to-4 demultiplexer, if the two select line C1 = 1 & C2 = 1, then the output will be _____

a) Y0 b) Y1

c) Y2 d) Y3

(xl) What is the indication of a short to ground in the output of a driving gate?

a) Only the output of the defective gate is affected b) There is a signal loss to all load gates

c) The node may be stuck in either the HIGH or the LOW state d) The affected node will be stuck in the HIGH state

(xli) The following switching functions are to be implemented using a decoder: f1 = ?m (1, 2, 4, 8, 10, 14), f2 = ?m (2, 5, 9, 11), f3 = ?m (2, 4, 5, 6, 7) The minimum configuration of decoder will be _____

a) 2 to 4 line
b) 3 to 8 line
c) 4 to 16 line
d) 5 to 32 line

(xlii) What is the function of an enable input on a multiplexer chip?

a) To apply Vcc
b) To connect ground
c) To active the entire chip
d) To active one half of the chip

(xliii) Minimum number of two input NAND gates required to realize XOR gate is

a) 3
b) 4
c) 5
d) 6

(xliv) The minimum number of 2-to-1 multiplexers required to realize a 32-to-1 multiplexer is

a) 31
b) 32
c) 16
d) 24

(xlv) The number of select lines for a 64– to – 1 multiplexer is

a) 3
b) 4
c) 5
d) 6

(xlvi) The expression Y=(A+B)(B+C)(C+A) shows

a) AND operation
b) POS operation
c) SOP operation
d) NAND operation

(xlvii) The binary representation of BCD number 00101001 is

a) 11101
b) 110101
c) 1101001
d) 101011

(xlviii) A binary-to-octal decoder is a

a) 3-line to 8-line decoder
b) 1-line to 8-line decoder
c) 4-line to 8-line decoder
d) None of these

(xlix) Flip-flops can be used to make

a) latches
b) bounce –elimination switches
c) registers
d) All of these

(l) A multiplexer is a

a) 1-to-N device
b) N-to-1 device
c) 1-to-1 device
d) N-to-N device

(li) A device which converts 2421 code into 8421 code is called a

a) code converter
b) code decoder
c) code encoder
d) coder

(lii) A binary number with n bits all of which are 1s has the value

a) $n^2 - 1$
b) 2^n
c) $2^{(n-1)}$
d) $2^n - 1$

(liii) 2's complement of 2's complement of the binary number 10110101 is

a) 1001010
b) 1001011
c) 10110101
d) 10111010

(liv) In a digital computer binary subtraction is performed

a) in the same way as we perform subtraction in decimal number system
b) using 2's complement method

c) using 9's complement method
d) using 10's complement method

(lv) ASCII code is a

a) 5-bit code
b) 7-bit code
c) 8-bit code
d) 10-bit code

(lvi) The difference output in a full-subtractor is the same as the

a) difference output of a half subtractor
b) sum output of a half adder
c) sum output of a full adder
d) carry output of a full adder

(lvii) How many inputs and outputs does a full-adder have ?

a) two inputs , two outputs
b) two inputs , one output
c) three inputs , two outputs
d) two inputs , three outputs

(lviii) How many full-adders are required to construct an m-bit parallel adder ?

a) m/2
b) m-1
c) m
d) m+1

(lix) In which of the following adder circuits is the carry ripple delay eliminated?

a) half-adder
b) full-adder
c) parallel adder
d) carry look ahead adder

(lx) The number of 3-line to 8-line decoders required for selecting 1 out of 64 is

a) 4
b) 8
c) 9
d) 16

(lxi) How many flip-flops are needed to divide the input frequency by 40?

a) 4
b) 5
c) 6
d) 40

(lxii) In sequential circuits the present input depends on

a) past inputs only
b) present inputs only
c) present as well as past inputs
d) past outputs

(lxiii) A mod-5 synchronous counter is designed using J-K flip-flops. the number of counts it will skip is

a) 2
b) 3
c) 5
d) 10

(lxiv) When an inventer is placed between the inputs of an S-R flip-flop, the resulting flip-flop is a

a) J-K flip-flop
b) master-slave flip-flop
c) T flip-flop
d) D flip-flop

(lxv) Master slave configuration is used in flip-flops to

a) increase its clocking rate
b) reduce power dissipation
c) eliminate race-round condition
d) improve its reliability

(lxvi) The primary advantage of RTL technology was that

a) It results as low power dissipation
b) It uses a minimum number of resistors
c) It uses a minimum number of transistors
d) It operates swiftly

(lxvii) The way to speed up DTL is to add an across intermediate resister is

a) Small “speed-up” capacitor
b) Small “speed-up” transistor
c) Large “speed-up” capacitor
d) Large ” speed-up” transistor

(lxviii) A disadvantage of DTL is

a) The input transistor to the resister
b) The input resister to the transistor
c) The increased fan-in
d) The increased fan-out

(lxix) Which logic is the fastest of all the logic families?

a) TTL
b) ECL
c) HTL
d) DTL

(lxx) ECL’s major disadvantage is that -

a) It requires more power
b) It’s fan-out capability is high
c) It creates more noise
d) It is slow