BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Bachelor of Science (Honours) in Computer Science

Course Name – Computer Architecture and Organization

Course Code - BCS302

Semester / Year - Semester III

Time allotted : 85 Minutes Full Marks : 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 70=70

1. *(Answer any Seventy)*

(i) A low memory can be connected to microprocessor by using

a) INTER b) RESET IN

c) INTER & RESET IN d) READY

(ii) A basic instruction that can be interpreted by a computer generally has

a) An operand and an address b) A decoder and an accumulator

c) Sequence register and decoder d) Program Counter

(iii) The addressing mode used in an instruction of the form ADD X, Y, is

a) absolute b) immediate

c) index d) indirect

(iv) Number of machine cycles required for RET instruction in 8085 microprocessor is

a) 1 b) 2

c) 3 d) 6

(v) In a microprocessor system, the RST instruction will cause an interrupt

a) only if an interrupt service routine is being executed b) only if a bit in the interrupt mask is made 0

c) only if interrupts have been enabled by an EI instruction

d) only when the processor is not working

(vi) In a generic microprocessor instruction cycle time is

a) Shorter than machine cycle time

b) Larger than machine cycle time

c) Ten times the machine cycle time

d) Exactly the same as the machine cycle time

(vii) The stack pointer in the microprocessor is a

a) 16 bit register that point to stack memory locations

b) 32 bit accumulator

c) memory location in the stack

d) flag register used for the stack

(viii) If we use 3 bits in the instruction word to indicate if an index register is to be used and if necessary, which one is to be used, then the number of index registers to be used in the machine will be

a) 3

b) 6

c) 5

d) 8

(ix) Pseudo-instructions are

a) Assembler directives

b) Instructions in any program that have corresponding machine code instruction

c) Instruction in any program whose absence will not change the output for any input

d) Program code

(x) The addressing mode used in the instruction ADD B is

a) Direct

b) Register

c) Register indirect

d) Index

(xi) The process of fetching and executing instructions, one at a time, in order of increasing address is called

a) Instruction execution
b) Straight line sequencing
c) Instruction fetch
d) Instruction Cycle

(xii) The ALU of a computer normally contains a number of high speed storage elements called

a) Semi-conductor memory
b) Registers
c) Hard disk
d) IC

(xiii) The unit of a computer system which executes program, communicates with and often controls the operation of other subsystems of the computer is the

a) CPU
b) Control unit
c) CPU & Control unit
d) Peripheral unit

(xiv) A source program is usually in _____

a) Assembly language
b) Machine level language
c) High-level language
d) Natural language

(xv) The control unit controls other units by generating _____

a) Control signals
b) Timing signals
c) Transfer signals
d) Command Signals

(xvi) The CISC stands for

a) Computer Instruction Set Compliment
b) Complete Instruction Set Compliment
c) Computer Indexed Set Components
d) Complex Instruction set computer

(xvii) A stack is a

a) 32-bit register in the microprocessor
b) 16-bit register in the microprocessor
c) set of memory locations in R/W memory reserved for storing information temporarily during the execution of a program
d) 16-bit memory address stored in the h program counter

(xviii) In the case of, Zero-address instruction method the operands are stored in _____

a) a) Registers
b) b) Accumulators
c) Push down stack
d) d) Cache

(xix) Zero-address instruction approach the data are stored in_____

a) Registers
b) Accumulator
c) Cache Memory
d) Push down Stack

(xx) In case of, One-address instruction method the operands are stored in_____

a) Registers
b) Accumulator
c) Push down Stack
d) Cache Memory

(xxi) Unit of computer which is capable of performing arithmetic, logical and data manipulation operations on binary numbers is called

a) CU
b) ALU
c) I/O Unit
d) Processing Unit

(xxii) In computer, ALU has

a) 2units
b) 3units
c) 4units
d) 5 units

(xxiii) When we perform subtraction on -7 and 1 the answer in 2's compliment form is _____

a) 1010
b) 1110
c) 110
d) 1000

(xxiv) The register used to store the flags is called as _____ .

a) Condition register
b) Status register
c) Test register
d) Log register

(xxv) What is the binary equivalent of the decimal number 368?

a) 101110000 b) 110110000

c) 111010000 d) 111100000

(xxvi) When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?

a) Sign-magnitude b) 1’s complement

c) 2’s complement d) 9’s complement

(xxvii) The chief reason why digital computers use complemented subtraction is that it

a) Simplifies the circuitry. b) Is a very simple process.

c) Can handle negative numbers easily. d) Avoids direct subtraction.

(xxviii) In a positive logic system, logic state 1 corresponds to

a) positive voltage b) higher voltage level

c) zero voltage level d) lower voltage level

(xxix) Divide overflow is generated when

a) Sign of the dividend is different from that of divisor. b) Sign of the dividend is same as that of divisor.

c) The first part of the dividend is smaller than the divisor. d) The first part of the dividend is greater than the divisor.

(xxx) A floating point number that has a 0 in the MSB of mantissa is said to have

a) Overflow b) Underflow

c) Important number d) Undefined

(xxxi) How can you represent a decimal point?

a) By a series of coefficients b) By weight decided by its position

c) By location as well as base

d) Either By weight decided by its position & By location as well as base

(xxxii) In subtraction of binary numbers, if the subtrahend digit is greater than the minuend, then borrow from a _____ significant bit.

a) Lower

b) Higher

c) First

d) Last

(xxxiii) Overflow occurs when

a) Data is out of range

b) Data is within range

c) Both Data is out of range &Data is within range

d) Neither Data is out of range & Data is within range

(xxxiv) When we perform subtraction on -8 and 2 the answer in 2's complement form is _____

a) 1010

b) 1110

c) 110

d) 1000

(xxxv) When we perform subtraction on -7 and -5 the answer in 2's complement form is _____

a) 11110

b) 10100

c) 10100

d) 100

(xxxvi) Which method/s of representation of numbers occupies a large amount of memory than others?

a) Sign-magnitude

b) 1's complement

c) 2's complement

d) 1's & 2's compliment

(xxxvii) The final addition sum of the numbers, 0111 & 0110 is _____

a) 1101

b) 1111

c) 1001

d) 1010

(xxxviii) In memory-mapped I/O…

a) The I/O devices and the memory share the same address space

b) The I/O devices have a separate address space

c) The memory and I/O devices have an associated address space

d) A part of the memory is specifically set aside for the I/O operation

(xxxix) The small extremely fast, RAM's are called as _____

a) RAM

b) Cache

c) Hard Disk

d) ROM

(xl) The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is

a) Exceptions

b) Signal handling

c) Interrupts

d) DMA

(xli) _____ is generally used to increase the apparent size of physical memory.

a) Secondary memory

b) Virtual memory

c) Hard-disk

d) Disks

(xlii) The main memory is structured into modules each with its own address register called _____

a) ABR

b) TLB

c) PC

d) IR

(xliii) The number failed attempts to access memory, stated in the form of a fraction is called as _____

a) Hit rate

b) Miss rate

c) Success rate

d) failure rate

(xliv) The next level of memory hierarchy after the L2 cache is _____

a) Secondary Storage

b) TLB

c) main memory
d) register

(xlv) he memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____

a) Level 1 cache
b) level 2 cache
c) register
d) TLB

(xlvi) A scheme in which portions of I/O address space are given to I/O devices, is called

a) Data mapped
b) Memory-mapped I/O
c) Backplane
d) Both Data mapped & Memory-mapped I/O

(xlvii) An instruction code must specify the address of the?

a) Operand
b) Opcode
c) Both of these
d) Register

(xlviii) If CPU and I/O interface share a common bus than transfer of data between two units is known as?

a) Asynchronous
b) Clock dependent
c) Synchronous
d) Decoder independent

(xlix) Which table handles store address of interrupt handling subroutine?

a) Vector table
b) Symbol link table
c) Interrupt vector table
d) PC

(l) How many RAM chips of size (256 K X 1 bit) are required to build 1M Memory?

a) 24
b) 4
c) 32
d) 8

(li) The main aim of virtual memory organization is _____

a) To provide effective memory access
b) To provide better memory transfer
c) To improve the execution of the program
d) All of these

(lii) Which of the following are true about associative memory? S1: Associative memory is fast memory S2: Associative memory searches by content and not by accessing the address

a) Both Associative memory is fast memory and Associative memory searches by content and not by accessing the address are true and Associative memory searches by content and not by accessing the address is correct explanation of Associative memory is fast memory
b) Both Associative memory is fast memory and Associative memory searches by content and not by accessing the address is not correct explanation of Associative memory is fast memory
c) Associative memory is fast memoryis true but Associative memory searches by content and not by accessing the address is false
d) Associative memory searches by content and not by accessing the address is true but Associative memory is fast memory is false

(liii) Dirty bit for a page in a page table

a) Helps avoid unnecessary writes on a paging device
b) Helps maintain LRU information
c) Allows only read on a page
d) Always use for 0 bit

(liv) Micro Instruction are kept in

a) Main memory
b) Control memory
c) Cache memory
d) Auxiliary memory

(lv) Which registers can interact with the secondary storage?

a) MAR
b) PC
c) IR
d) R0

(lvi) The method of mapping the consecutive memory blocks to consecutive

cache blocks is called _____

a) Set associative
b) Associative
c) Direct
d) Indirect

(lvii) The memory blocks are mapped on to the cache with the help of _____

a) Hash functions
b) Vectors
c) Mapping functions
d) Register

(lviii) The smallest entity of memory is called _____

a) Cell
b) Block
c) Instance
d) Unit

(lix) A term for simultaneous access to a resource, physical or logical.

a) Multiprogramming
b) Multitasking
c) Threads
d) Concurrency

(lx) A parallelism based on increasing processor word size.

a) instructional
b) bit level
c) bit based
d) increasing

(lxi) CPU does not perform the operation.....

a) data transfer
b) logic operation
c) arithmetic operation
d) all of these

(lxii) From where interrupts are generated?

a) Central processing unit
b) Memory chips
c) Registers
d) I/O devices

(lxiii) Which of the following bus is used to transfer data from main memory to peripheral device?

a) DMA Bus
b) Output bus

c) Data bus
d) Input bus

(lxiv) PC Program Counter is also called

a) instruction pointer
b) memory pointer
c) file pointer
d) data counter

(lxv) The internal components of the processor are connected by _____

a) Processor intra-connectivity circuitry
b) Processor bus
c) Memory bus
d) Rambus

(lxvi) Which method of representation has two representations for ‘0’?

a) Sign-magnitude
b) 1’s complement
c) 2’s complement
d) Both Sign-magnitude and 1’s complement

(lxvii) Which determines the address of I/O interface?

a) Register select
b) Chip select
c) Both of these
d) Neither Register select or Chip select

(lxviii) Whenever CPU detects an interrupt, what it do with current state?

a) Save it
b) Discard it
c) Depends system to system
d) First finish it

(lxix) The decoded instruction is stored in _____

a) IR
b) PC
c) Registers
d) MDR

(lxx) An interrupt in which the external device supplies its address as well as the interrupt requests is known as

a) Vectored interrupt
b) Maskable interrupt
c) Non maskable interrupt
d) Designated Interrupt