BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Bachelor of Technology in Computer Science & Engineering

Course Name – Digital Electronics

Course Code - BCSE301

Semester / Year - Semester III

Time allotted : 85 Minutes Full Marks : 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 70=70

1. *(Answer any Seventy)*

(i) Karnaugh map is used:

a) To draw the digital circuit layout
b) To simplify logical function
c) To locate different gates in a digital circuit
d) None of these

(ii) How many AND gates are required for a 8-to-1 multiplexer?

a) 5
b) 7
c) 8
d) 6

(iii) The number 140 in octal is equivalent to?

a) $(90)_{10}$
b) $(88)_{10}$
c) $(86)_{10}$
d) $(96)_{10}$

(iv) In witch of the following base systems is 123 not a valid number?

a) Base16
b) Base3
c) Base10
d) Base8

(v) The expression Y=AB+BC+AC shows the _____ operation.

a) SOP
b) NOR
c) POS
d) EX-OR

(vi) Full subtractor is used to perform subtraction of _____.

a) 4 bits
b) 3 bits
c) 2 bits
d) 8 bits

(vii)

The value of base x is: $(211)_x = (152)_8$

a) 7
b) 8
c) 6
d) 5

(viii) Before an SOP implementation, the expression X= AB(C'D+EF) would require a total of how many gates?

a) 1
b) 2
c) 4
d) 5

(ix) Which is the prohibited state/ condition in S-R latch and needs to be avoided due to unpredictable nature of output?

a) S = R = 0
b) S = 0, R = 1
c) S = 1, R = 0
d) S = R = 1

(x) Which type of triggering is shown by the D flip flops in buffer registers for the temporary storage of digital words?

a) Positive level triggering
b) Negative level triggering
c) Positive edge triggering
d) Negative edge triggering

(xi)

In 1:4 demultiplexer, if $S_0 = 1$ & $S_1 = 1$, then the output will be _____.

a) b)

Y_0 Y_1

c) d)

Y_2 Y_3

(xii)

The decimal equivalent of the binary number $(1011.011)_2$ is _____.

a) b)

$(11.375)_{10}$ $(10.123)_{10}$

c) d)

$(11.175)_{10}$ $(9.23)_{10}$

(xiii) The largest two digit hexadecimal number is _____.

a) b)

$(FE)_{16}$ $(FD)_{16}$

c) d)

$(FF)_{16}$ $(EF)_{16}$

(xiv) The Boolean function A + BC is a reduced form of _____.

a) AB + BC b) (A + B)(A + C)

c) A'B + AB'C d) (A + C)B

(xv) The expression Y=(A+B)(B+C)(C+A) shows the _____ operation.

a) AND b) POS

c) SOP d) NAND

(xvi) Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?

a) OR gates only
b) AND gates and NOT gates
c) AND gates, OR gates, and NOT gates
d) OR gates and NOT gates

(xvii) In a combinational circuit, the output at any time depends only on the _____ at that time.

a) Voltage
b) Intermediate values
c) Input values
d) Clock pulses

(xviii) In a sequential circuit, the output at any time depends only on the input values at that time.

a) Past output values
b) Past output and Present input
c) Intermediate values
d) Present input values

(xix) In parts of the processor, adders are used to calculate _____.

a) Addresse
b) Table indices
c) Increment and decrement operators
d) All of these

(xx) TTL is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by _____.

a) Resistors
b) Bipolar junction transistors
c) One transistor
d) Resistors and transistors respectively

(xxi) How many stages a DTL consist of?

a) 2
b) 3
c) 4
d) 5

(xxii) How many NOT gates are required to implement the Boolean expression: X = AB’C + A’BC?

a) 2
b) 3

c) 4 d) 5

(xxiii)

If the number of n selected input lines is equal to 2^m then it requires _____ select lines.

a) 2 b) m

c) n d) 2n

(xxiv) The full form of ECL is _____.

a) Emitter-collector logic b) Emitter-complementary logic

c) Emitter-coupled logic d) Emitter-cored logic

(xxv) If A, B and C are the inputs of a full adder then the carry is given by _____

a) A AND B OR (A OR B) AND C b) A OR B OR (A AND B) C

c) (A AND B) OR (A AND B)C d) A XOR B XOR (A XOR B) AND C

(xxvi) Half subtractor is used to perform subtraction of _____.

a) 2 bits b) 3 bits

c) 4 bits d) 5 bits

(xxvii) The full subtractor can be implemented using _____.

a) Two XOR and an OR gates b) Two half subtractors and an OR gate

c) Two multiplexers and an AND gate d) Two comparators and an AND gate

(xxviii) In an ECL the output is taken from _____.

a) Emitter b) Base

c) Collector d) Junction of emitter and base

(xxix) Which gates are ideal for checking the parity bits?

a) AND
b) NAND
c) EX-OR
d) EX-NOR

(xxx) When a high is applied to the Set line of an SR latch, then _____.
a) Q output goes high
b) Q' output goes high
c) Q output goes low
d) Both Q and Q' go high

(xxxi) Which of the following is the Universal Flip-flop?
a) S-R flip-flop
b) J-K flip-flop
c) Master slave flip-flop
d) D Flip-flop

(xxxii) A NAND based S'-R' latch can be converted into S-R latch by placing _____.
a) A D latch at each of its input
b) A D latch at each of its input
c) It can never be converted
d) Both a D latch and an inverter at its input

(xxxiii) Ripple counters are also called _____.
a) SSI counters
b) Asynchronous counters
c) Synchronous counters
d) VLSI counters

(xxxiv) (A + B)(A' * B') = ?
a) 1
b) 0
c) AB
d) AB'

(xxxv) The excess-3 code for 597 is given by _____.
a) 100011001010
b) 100010100111
c) 10110010111
d) 10110101101

(xxxvi)

On subtracting $(001100)_2$ from $(101001)_2$ using 2's complement, we get

_____.

a) 1101100
b) 011101
c) 11010101
d) 11010111

(xxxvii)

On subtracting $(01010)_2$ from $(11110)_2$ using 1's complement, we get _____.

a) 1001
b) 11010
c) 10101
d) 10100

(xxxviii) The expression for Absorption law is given by _____

a) A + AB = A
b) A + AB = B
c) AB + AA' = A
d) A + B = B + A

(xxxix) A 3-variable Karnaugh map has _____.

a) 9 cells
b) 8 cells
c) 4 cells
d) 16 cells

(xl) In a multiplexer the output depends on its _____.

a) Data inputs
b) Select inputs
c) Select outputs
d) None of these

(xli) When two 16-input multiplexers drive a 2-input MUX, what is the result?

a) 2-input MUX
b) 4-input MUX
c) 16-input MUX
d) 32-input MUX

(xlii) The decimal equivalent of hex number 1A53 is_____.

a) 6793
b) 6739
c) 6973
d) 6379

(xliii)

$(734)_8 = (?)_{16}$

a) C1D
b) DC1
c) 1CD
d) 1DC

(xliv) When an input signal A=11001 is applied to a NOT gate serially, its output signal is

a) 111
b) 00110
c) 10101
d) 11001

(xlv) The result of adding hexadecimal number A6 to 3A is_____.

a) DD
b) E0
c) F0
d) EF

(xlvi) One multiplexer can take the place of

a) Several SSI logic gates
b) Combinational logic circuits
c) Several Ex-NOR gates
d) Several SSI logic gates or combinational logic circuits

(xlvii) How many shift registers are used in a 4-bit serial adder?

a) 2
b) 3
c) 4
d) 5

(xlviii) ECL's major disadvantage is that

a) It requires more power
b) It's fan-out capability is high
c) It creates more noise
d) It is slow

(xlix) In Boolean algebra, the OR operation is performed by which properties

a) Associative properties
b) Commutative properties
c) Distributive properties
d) All of these

(l) Which is an incorrect rule of binary subtraction from the following?

a) 0 – 0 = 0
b) 0 – 1 = -1
c) 1 – 0 = 1
d) 0 – 1 = 1 with borrow '1'

(li)

Binary subtraction of 100101 – 011110 is

a) 000111
b) 10101
c) 111000
d) 101010

(lii) Perform multiplication of the binary numbers: 01001 × 01011 = ?

a) 001100011
b) 110011100
c) 10100110
d) 101010111

(liii) There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and _____ operations.

a) X-NOR
b) X-OR
c) NOR
d) NAND

(liv) If A and B are the inputs of a half adder, the sum is given by

a) A AND B
b) A OR B
c) A XOR B
d) A EX-NOR B

(lv) When performing subtraction by addition in the 2's-complement system

a) The minuend and the subtrahend are both changed to the 2's-complement
b) The minuend is changed to 2's-complement and the subtrahend is left in its original form
c) The minuend is left in its original form and the subtrahend is changed to its 2's-complement
d) The minuend and subtrahend are both left in their original form

(lvi) Standard TTL circuits operate with a __ volt power supply

a) 2 b) 5
c) 4 d) 6

(lvii) In RTL NOR gate, the output is at logic 1 only when all the inputs are at
a) logic 0 b) logic 1
c) +10V d) Floating

(lviii) The primary advantage of RTL technology was that
a) It results as low power dissipation b) It uses a minimum number of resistors
c) It uses a minimum number of transistors d) It operates swiftly

(lix) TTL circuits with “totem-pole” output stage minimize
a) The power dissipation in RTL b) The time consumption in RTL
c) The speed of transferring rate in RTL d) Propagation delay in RTL

(lx) The way to speed up DTL is to add an across intermediate resister is
a) Small “speed-up” capacitor b) Small “speed-up” transistor
c) Large “speed-up” capacitor d) Large ” speed-up” transistor

(lxi) A digital multiplexer is a combinational circuit that selects
a) One digital information from several sources and transmits the selected one b) Many digital information and convert them into one
c) Many decimal inputs and transmits the selected information d) Many decimal outputs and accepts the selected information

(lxii) The selector inputs to an arithmetic/logic unit (ALU) determine the
a) Selection of the IC b) Arithmetic or logic function
c) Data word selection d) Clock frequency to be used

(lxiii) The minimum and maximum number of transistors can be used by 2 input AND gate is

a) 2 & 3
b) 3 & 2
c) 4 & 5
d) 5 & 4

(lxiv) The basic R-S flip-flop is

a) A monostable multivibrator
b) A bistable multivibrator
c) An astable multivibrator
d) A Schmitt trigger

(lxv) Which of the following circuits come under the class of combinational logic circuits? 1. Full adder 2. Full subtractor 3. Half adder 4. J-K flip 5. Counter

a) 1 only
b) 3 and 4
c) 4 and 5
d) 1, 2 and 3

(lxvi) If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____

a) SET
b) RESET
c) Clear
d) Invalid

(lxvii) One example of the use of an S-R flip-flop is as _____

a) Transition pulse generator
b) Racer
c) Switch debouncer
d) Astable oscillator

(lxviii) A 4-bit shift register that receives 4 bits of parallel data will shift to the _____ by _____ position for each clock pulse.

a) Right, one
b) Right, two
c) Left, one
d) Left, three

(lxix) A ripple counter’s speed is limited by the propagation delay of _____

a) Each flip-flop
b) All flip-flops and gates
c) The flip-flops only with gates
d) Only circuit gates

(lxx) Which of the following circuit can be used as serial to parallel converter?

a) Multiplexer
b) Demultiplexer
c) Decoder
d) Digital counter