BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Bachelor of Technology in Computer Science & Engineering

Course Name – Computer Organization and Architecture

Course Code - BCSE303

Semester / Year - Semester III

Time allotted : 85 Minutes Full Marks : 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 70=70

1. *(Answer any Seventy)*

(i) If the searched data is found in the desired memory, it is said to be

a) hit ratio b) miss

c) hit d) hit rate

(ii) 2's complement of 10101011:

a) 1010101 b) 1011101

c) 1110101 d) 11010101

(iii) Babbage's difference engine is a computer

a) for Subtraction b) for both addition and subtraction

c) for performing multi step operations automatically d) for arithmetic and logical operation

(iv) The fastest data access can be obtained using

a) SRAM b) DRAM

c) Cache d) Register

(v) Booth's Algorithm is applied on _____

a) decimal numbers b) binary numbers

c) hexadecimal numbers d) octal Numbers

(vi) Instruction Cycle is

a) fetch-decode-execution
b) fetch-execution decode
c) decode-fetch-execution
d) none of these

(vii) In computers, subtraction is generally carried out by

a) 9’s complement
b) 10’s complement
c) 1’s complement
d) 2’s complement

(viii) The 2s compliment form (Use 6 bit word) of the number 1010 is

a) 111100
b) 110110
c) 110111
d) 1011

(ix) Which of the following is an exclusive form of OR logic gate?

a) NOR
b) XNOR
c) OR
d) XOR

(x) RISC stands for

a) Remodeled Interface System Computer
b) Remote Intranet Secured Connection
c) Reduced Instruction Set Computer
d) Runtime Instruction Set Compiler

(xi) In which cycle the memory is read and the contents of memory at the address contained in the PC register are loaded into Instruction Register

a) Execution Cycle
b) Memory Cycle
c) Decode Cycle
d) Fetch Cycle

(xii) The sequence of operations performed by CPU in processing an instruction is

a) Execution cycle
b) Fetch cycle
c) Decode
d) Instruction cycle

(xiii) Micro instructions are kept in the

a) main memory
b) cache memory
c) control memory
d) none of these

(xiv) Two important fields of an instruction are

a) Opcode
b) Operand
c) Only Opcode
d) Both Opcode and Operand

(xv) How many bits are needed to represent a digit in hexadecimal notation?

a) 8
b) 16
c) 4
d) 2

(xvi) The 2s compliment of the number 101010 is

a) 10101
b) 110010
c) 110101
d) 10110

(xvii) Which one of following is volatile in nature

a) CD-ROM
b) ROM
c) DVD-ROM
d) RAM

(xviii) Subtractor can be implemented using

a) adder
b) complementer
c) both adder and complementer
d) none of these

(xix) Any electronic holding place where data can be stored and retrieved later whenever required is _____

a) Memory
b) Drive
c) Disk
d) Circuit

(xx) The slowest and last on the hierarchy scale of memory devices is

a) Main memory
b) Secondary memory
c) Flash drive
d) Cache

(xxi) Which of the following is used to store the address of next instruction

a) Accumulator
b) MAR
c) Program Counter
d) MDR

(xxii) Floating point representation is used to store

a) Boolean values
b) Whole numbers
c) Real integers
d) Integers

(xxiii) Which of the following has smallest capacity

a) cache memory
b) RAM
c) secondary memory
d) registers

(xxiv) Cache memory acts between

a) CPU and RAM
b) CPU and registers
c) RAM and ROM
d) None of these

(xxv) Cache memory works on the principle of

a) Locality of reference
b) Locality of memory
c) Locality of data
d) Locality of data and memory

(xxvi) Memory unit accessed by content is called

a) ROM
b) Virtual memory
c) Programmable memory
d) Associative memory

(xxvii) Instruction pipeline can be implemented by means of

a) LIFO buffer
b) Stack
c) FIFO buffer
d) None of these

(xxviii) An address in main memory is called

a) Physical address
b) Logical address

c) Memory address
d) Word address

(xxix) If the value V(x) of the target operand is contained in the address field itself, the addressing mode is

a) immediate
b) direct
c) indirect
d) implied

(xxx) A register capable of shifting its binary information either to the right or the left is called a

a) parallel register
b) serial register
c) shift register
d) storage register

(xxxi) In which addressing mode the operand is given explicitly in the instruction

a) Absolute
b) Immediate
c) Indirect
d) Direct

(xxxii) Associative memory is

a) Very cheap memory
b) pointer addressable memory
c) Content addressable memory
d) Slow memory

(xxxiii) Program always deals with

a) logical address
b) absolute address
c) physical address
d) relative address

(xxxiv) Which one of the following is the address generated by CPU?

a) physical address
b) absolute address
c) logical address
d) relative address

(xxxv) CPU fetches the instruction from memory according to the value of

a) program counter
b) instruction register

c) status register
d) program status word

(xxxvi) Cache memory-

a) has greater capacity than RAM
b) is faster to access than CPU Registers
c) is permanent storage
d) faster to access than RAM

(xxxvii) Which of the following is used to hold the memory location of data needs to be accessed

a) Accumulator
b) MAR
c) MDR
d) Program Counter

(xxxviii) The addressing mode, where the operand value is implicitly specified

a) implied
b) direct
c) immediate
d) indirect

(xxxix) Which of the following addressing mode is used for the instruction "PUSH B"?

a) Register
b) Register indirect
c) Direct
d) Immediate

(xl) The user view of memory is supported by

a) paging
b) segmentation
c) both
d) none

(xli) The minimum number of operand with any instruction is

a) 1
b) 0
c) 2
d) 3

(xlii) Data hazards occur when

a) Greater performance loss
b) Machine size is limited
c) Some functional unit is not fully
d) Pipeline changes the order of read/write

pipelined

access to operands

(xliii) The difference circuit in full subtractor is implemented using

a) XOR

b) OR

c) AND

d) NOT

(xliv) The average time required to reach a storage location in memory and obtain its contents is called

a) Latency time

b) Access time

c) Turnaround time

d) Response time

(xlv) The device which is used to connect a peripheral to a bus is called

a) Control Register

b) Interface

c) Communication Protocol

d) None of these

(xlvi) If M denotes the number of memory locations and N denotes the word size, then an expression that denotes the storage capacity is _____.

a) M*N

b) M+N

c) 2M+N

d) 2M-N

(xlvii) Which of the following is independent of the address bus?

a) Secondary Memory

b) Main Memory

c) Onboard Memory

d) Cache Memory

(xlviii) A systemwith 32 registers, the register id is _____ long.

a) 16 bit

b) 8 bits

c) 5 bits

d) 6 bits

(xlix) The step during which a new instruction is read from the memory

a) decode

b) fetch

c) execute

d) none of these

(l) BR signal in DMA stands for

a) bus record
b) bus register
c) bus request
d) buffer register

(li) The signal sent by the CPU to the DMA controller to take control over buses

a) BG
b) ACK
c) BR
d) DMA

(lii) In which addressing mode the address of the operand is specified

a) Absolute
b) Immediate
c) Indirect
d) Direct

(liii) The signal sent by the DMA controller to the CPU, requesting to take control over buses for data transfer

a) BG
b) ACK
c) BR
d) DMA

(liv) A microporgram is sequencer perform the operation

a) write
b) execute
c) read and write
d) read and execute

(lv) Which of the architecture is power efficient?

a) CISC
b) RISC
c) ISA
d) IANA

(lvi) Partition of memory in fixed size is

a) Segmentation
b) paging
c) both segmentation and paging
d) neither segmentation nor paging

(lvii) The usual BUS structure used to connect the I/O devices is _____

a) Star BUS structure
b) Multiple BUS structure
c) Single BUS structure
d) Node to Node BUS structure

(lviii) SIMD stands for

a) Single instruction memory data
b) Single information multiple data
c) Sequence information multiple data
d) Single instruction multiple data

(lix) The decoded instruction is stored in _____

a) IR
b) PC
c) Registers
d) MDR

(lx) Processors of all computer, whether micro, mini or mainframe must have

a) ALU
b) Control unit
c) primary storage
d) All of the options.

(lxi) A stack is

a) a 8-bit register in the microprocessor
b) a 16-bit register in the microprocessor
c) a set of memory locations in R/WM reserved for storing information temporarily during the execution of computer
d) a 16-bit memory address stored in the program counter

(lxii) Interrupts which are initiated by an instruction are

a) internal
b) external
c) hardware
d) software

(lxiii) The average time required to access a data in given memory locations is

a) seek time
b) access time
c) turnaround time
d) transfer time

(lxiv) The _____ format is usually used to store data.

a) BCD
b) Decimal
c) Hexadecimal
d) Octal

(lxv) The 8-bit encoding format used to store data in a computer is _____

a) ASCII
b) EBCDIC
c) ANCI
d) USCII

(lxvi) DRAM is used as main memory because it

a) consumes less power
b) has high speed
c) has lower cell density
d) needs refreshing circuitry

(lxvii) The control unit controls other units by generating _____

a) Control Signals
b) Timing Signals
c) Transfer Signals
d) Command Signals

(lxviii) _____ bus structure is usually used to connect I/O devices.

a) Single Bus
b) Multiple Bus
c) Star Bus
d) Rambus

(lxix)

Maximum n bit 2 s complement number is

a) 2^n

b) 2^{n-1}

c) $2^{n-1} - 1$

d) cannot said

(lxx)

BCD uses binary number system to specify decimal numbers

a)

1-10

b)

1-9

c)

0-9

d)

0-10