BRAINWARE UNIVERSITY

Term End Examination 2020 - 21

Programme – Bachelor of Science (Honours) in Advanced Networking & Cyber Security

Course Name – Computer Organization and Architecture

Course Code - BNCSC303

Semester / Year - Semester III

Time allotted : 75 Minutes Full Marks : 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 60=60

1. *(Answer any Sixty)*

(i) Equivalent of the hexadecimal number 12AE516 in decimal is

a) 12345 b) 76517

c) 12AB5 d) 101011

(ii) Convert binary 100110101 to octal results

a) 11001010 b) 456

c) 465 d) 4F

(iii) The 2’s complement representation of decimal (-1) is

a) 11 b) 1111

c) 1 d) Both 11 and 1111

(iv) A full adder is a combinational circuit that performs

a) The arithmetic sum of three bits. b) The arithmetic sum of two bits

c) The logical OR operation d) Multiplication of two numbers

(v) The subtraction operation can be implemented with the help of binary adder circuit, because

a) A-B=A+B b) A-B=A+(-B)

c) A-B=B-A d) A-B=A-(-B)

(vi) ASCII stands for

a) American Standard Code for Information Interchange

b) Arithmetic Standard Code for Information Interchange

c) American Source Code for Information Interchange

d) American Standard Code for input Interface

(vii) Disadvantage of carry propagate adder is-

a) The addition delay becomes large, if the sizes of the numbers to be added are large.

b) Hardware cost is more than building of a serial adder

c) Unavailability of suitable hardware

d) Both The addition delay becomes large, if the sizes of the numbers to be added are large and Hardware cost is more than building of a serial adder

(viii) Any signed negative binary number is recognized by its _____

a) MSB

b) LSB

c) Byte

d) Nibble

(ix) The representation of octal number (532.2)8 in decimal is _____

a) (346.25)10

b) (532.864)10

c) (340.67)10

d) (531.668)10

(x) (A + B)(A’ * B’) = ?

a) 1

b) 0

c) AB

d) AB’

(xi) How many truth table entries are necessary for a four-input circuit?

a) 4

b) 8

c) 12

d) 16

(xii) Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?

a) OR gates only
b) AND gates and NOT gates
c) AND gates, OR gates, and NOT gates
d) OR gates and NOT gates

(xiii) Total number of inputs in a half adder is _____

a) 2
b) 3
c) 4
d) 1

(xiv) What is the minimum number of two-input NAND gates used to perform the function of two input OR gate ?

a) One
b) two
c) three
d) four

(xv) Which of the following gates would output 1 when one input is 1 and other input is 0 ?

a) OR gate
b) AND gate
c) NAND gate
d) both OR gate and NAND gate

(xvi) The term RISC may refers to-

a) Reference Instruction Set Computer
b) Remote Instruction Set Computer
c) Register Instruction Set Computer
d) Reduced Instruction Set Computer

(xvii) Accumulator based CPU organization is a

a) Simple CPU organization, in which the accumulator is used to control the registers
b) Simple CPU organization, in which the accumulator is used as the program counter
c) Simple CPU organization, in which the accumulator register is used implicitly to process instructions
d) Simple CPU organization, in which the accumulator register is used to store the complete program

(xviii) Register direct addressing mode instruction ADD R1, R2

a) adds the contents of the register R1 & R2 and store the result in R1
b) adds the contents of the register R1 & R2 and store the result in primary memory
c) adds the contents of the register R1 & R2
d) adds the contents of the register R1 & R2

and store the result in R2

and store the result in both R1 and R2

(xix) In indexed addressing mode

a) The contents of the index register is added to the primary memory contents to produce the effective address

b) The content of the program counter is added to the index register to produce the effective address

c) The content of the index register moved to the processor to produce the effective address

d) The contents of the index register is added to the address part of the instruction to produce the effective address

(xx) Number of registers are present in RISC architecture are-

a) stack based memory, no registers are installed

b) one, single register called the accumulator

c) very few in numbers

d) many symmetric registers, organized in a register file.

(xxi) Stack Based CPU Organization follows

a) two address length instruction

b) one address length instruction

c) zero address length instruction

d) three address length instruction

(xxii) In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____

a) EA = 5+R1

b) EA = R1

c) EA = [R1]

d) EA = 5+[R1]

(xxiii) In the case of, Zero-address instruction method the operands are stored in _____

a) Registers

b) Accumulators

c) Push down stack

d) Cache

(xxiv) The addressing mode which makes use of in-direction pointers is _____

a) Indirect addressing mode

b) Index addressing mode

c) Relative addressing mode
d) Offset addressing mode

(xxv) Which representation is most efficient to perform arithmetic operations

a) Sign-magnitude
b) 1's complement
c) 2'S complement
d) None of the mentioned

(xxvi) Which method of representation has two representations for '0'?

a) Sign-magnitude
b) 1's complement
c) 2's complement
d) None of the mentioned

(xxvii) The addressing mode/s, which uses the PC instead of a general purpose register is _____

a) Indexed with offset
b) Relative
c) Direct
d) Both Indexed with offset and direct

(xxviii) The addressing mode, where you directly specify the operand value is _____

a) Immediate
b) Direct
c) Definite
d) Relative

(xxix) In a data hazard, when the current instruction must wait to read data until after a previous instruction writes the correct data.

a) WAW (write after write) hazards
b) RAR (read after read) hazards
c) WAR (write after read) hazards
d) RAW (read after write) hazards

(xxx) In a data hazard, when the current instruction must wait to write data until after a previous instruction writes to the same register is called

a) WAW (write after write) hazard
b) RAW (read after write) hazards
c) WAR (write after read) hazards
d) RAR (read after read) hazards

(xxxi) DMA-transfer may be categorized into

a) Burst transfer & cycle stealing
b) I/O transfer & Data copy
c) Input data & output result
d) Memory transfer & data write

(xxxii) The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is

a) Exceptions
b) Signal handling
c) Interrupts
d) DMA

(xxxiii) The method which offers higher speeds of I/O transfers is

a) Interrupts
b) Memory mapping
c) Program-controlled I/O
d) DMA

(xxxiv) The interrupt-request line is a part of the

a) Data line
b) Control line
c) Address line
d) None of these

(xxxv) The return address from the interrupt-service routine is stored on the

a) System heap
b) Processor register
c) Processor stack
d) Memory

(xxxvi) The DMA transfers are performed by a control circuit called as _____

a) Device interface
b) DMA controller
c) Data controller
d) Overlooker

(xxxvii) Interrupts initiated by an instruction is called as _____

a) Internal
b) External
c) Hardware
d) Software

(xxxviii) The primary function of the BUS is _____

a) To connect the various devices to the cpu
b) To provide a path for communication

between the processor and other devices

c) To facilitate data transfer between various devices

d) All of the mentioned

(xxxix) The classification of BUSes into synchronous and asynchronous is based on _____

a) The devices connected to them

b) The type of data transfer

c) The Timing of data transfers

d) None of the mentioned

(xl) The device which starts data transfer is called _____

a) Master

b) Transactor

c) Distributor

d) Initiator

(xli) The device which interacts with the initiator is _____

a) Slave

b) Master

c) Responder

d) Friend

(xlii) Which is fed into the BUS first by the initiator?

a) Data

b) Address

c) Commands or controls

d) Address, Commands or controls

(xliii) The best mode of connection between devices which need to send or receive large amounts of data over a short distance is _____

a) BUS

b) Serial port

c) Parallel port

d) Isochronous port

(xliv) he output of the encoder circuit is/are _____

a) ASCII code

b) ASCII code and the valid signal

c) Encoded signal

d) None of the mentioned

(xlv) In terms of power consumption, SRAM type memories requires

a) No power supply

b) constant power supply, which indicates SRAM types of memories consumes more power;

c) reduced power consumption, because the information is stored in a capacitor

d) Controlled power consumption, because the power is controlled with a switch

(xlvi) A large primary memory can be constructed by expanding some small size chips in vertically, where

a) Number of location is increased

b) Size of the word is increased

c) Size of the word is decreased

d) Number of location is decreased.

(xlvii) CDRAM type memory may refers to

a) A special type of random access memory with a built in cache to provide a high speed buffer for the main portion of DRAM

b) a CD that can be read by a computer with an optical drive

c) a CD to install programs in a RAM

d) A special RAM for CD drives

(xlviii) One of the memory accessing method is random access, which

a) is the combination of sequential access and random access method

b) Accessed in a linear sequential manner

c) is a special type of random access that enables one to make a comparison between bit locations within a word for a specific match

d) may be accessed randomly for any location of the memory

(xlix) In magnetic tapes, each frame is assigned

a) To store 9 bit of data. The first 8 bits forms a data byte, whereas the 9th bit holds the parity bit.

b) To store 1 byte data. The first 7 bits forms a data word, whereas the 8th bit holds the sign bit.

c) To store 9 bit of data. The first bit forms a data, whereas the remaining bits holds the parity bits.

d) To store a single bit data

(l) One of the memory accessing method is direct access, which

a) is the combination of sequential access and random access method

b) Accessed in a linear sequential manner

c) is a special type of random access that enables one to make a comparison between bit locations within a word for a specific match

d) may be accessed randomly for any location of the memory

(li) One of the memory accessing method is associative access, which

a) is the combination of sequential access and random access method

b) Accessed in a linear sequential manner

c) is a special type of random access that enables one to make a comparison between bit locations within a word for a specific match

d) may be accessed randomly for any location of the memory

(lii) EEPROM may stands for

a) Electrically Expandable Programmable Read Only Memory

b) Electrically Erasable Programmable Read Only Memory

c) Erasable And Executable Programmable Read Only Memory

d) Effectively Expandable Programmable Read Only Memory

(liii) The cells in a row are connected to a common line called _____

a) Work line

b) Word line

c) Length line

d) Principle diagonal

(liv) The cells in each column are connected to _____

a) Word line

b) Data line

c) Read line

d) Sense/ Write line

(lv) Which is the last on the hierarchy scale of memory devices?

a) Main memory

b) Secondary memory

c) TLB
d) Flash drives

(lvi) In set-associative technique, the blocks are grouped into _____ sets

a) 4
b) 8
c) 12
d) 6

(lvii) The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____

a) Set associative
b) Associative
c) Direct
d) Indirect

(lviii) In _____ protocol the information is directly written into the main memory

a) Write through
b) Write back
c) Write first
d) None of the mentioned

(lix) During a write operation if the required block is not present in the cache then _____ occurs.

a) Write latency
b) Write hit
c) Write delay
d) Write miss

(lx) 16 X 8 Organisation of memory cells, can store upto _____

a) 256 bits
b) 1024 bits
c) 512 bits
d) 128 bits