# BRAINWARE UNIVERSITY

## Term End Examination 2020 - 21

**Programme – Diploma in Electronics & Communication Engineering**

**Course Name – Microcontroller and Embedded System**

**Course Code - DECE503**

**Semester / Year - Semester V**

Time allotted : 85 Minutes | Full Marks : 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

## Group-A

(Multiple Choice Type Question) 1 x 70=70

1. *(Answer any Seventy )*

(i) A microcontroller at-least should consist of:

a) RAM, ROM, I/O devices, serial and parallel ports and timers

b) CPU, RAM, I/O devices, serial and parallel ports and timers

c) CPU, RAM, ROM, I/O devices, serial and parallel ports and timers

d) CPU, ROM, I/O devices and timers

(ii) What is the order decided by a processor or the CPU of a controller to execute an instruction?

a) decode,fetch,execute

b) execute,fetch,decode

c) fetch,execute,decode

d) fetch,decode,execute

(iii) How are the performance and the computer capability affected by increasing its internal bus width?

a) it increases and turns better

b) it decreases

c) remains the same

d) internal bus width doesn't affect the performance in any way

(iv) Give the names of the buses present in a controller for transferring data from one place to another?

a) data bus, address bus

b) data bus

c) data bus, address bus, control bus

d) address bus

(v) What is the most appropriate criterion for choosing the right microcontroller of our choice?

a) speed
b) availability
c) ease with the product
d) all of the mentioned

(vi) How many types of architectures are available, for designing a device that is able to work on its own?

a) 3
b) 2
c) 1
d) 4

(vii) Which architecture involves both the volatile and the non volatile memory?

a) Harvard architecture
b) Von Neumann architecture
c) None of the mentioned
d) All of the mentioned

(viii) Which out of the following supports Harvard architecture?

a) ARM7
b) Pentium
c) SHARC
d) All of the mentioned

(ix) Which of the following supports CISC as well as Harvard architecture?

a) ARM7
b) ARM9
c) SHARC
d) None of the mentioned

(x) 8051 series of microcontrollers are made by which of the following companies?

a) Atmel
b) Philips
c) Atmel & Philips
d) None of the mentioned

(xi) 8051 series has how many 16 bit registers?

a) 2
b) 3
c) 1
d) 0

(xii) When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected?

a) PSW
b) SP
c) DPTR
d) PC

(xiii) On power up, the 8051 uses which RAM locations for register R0- R7

a) 00-2F
b) 00-07
c) 00-7F
d) 00-0F

(xiv) The example of output device is

a) CRT display
b) 7-segment display
c) Printer
d) All of the mentioned

(xv) The operation, IOWR (active low) performs

a) write operation on input data
b) write operation on output data
c) read operation on input data
d) read operation on output data

(xvi) While performing read operation, one must take care that much current should not be

a) sourced from data lines
b) sinked from data lines
c) sourced or sinked from data lines
d) sinked from address lines

(xvii) The chip 74LS245 is

a) bidirectional buffer
b) 8-bit input port
c) one that has 8 buffers
d) all of the mentioned

(xviii) In memory-mapped scheme, the devices are viewed as

a) distinct I/O devices
b) memory locations
c) only input devices
d) only output devices

(xix) A machine language instruction format consists of

a) Operand field
b) Operation code field
c) Operation code field & operand field
d) none of the mentioned

(xx) The instruction "JUMP" belongs to

a) sequential control flow instructions
b) control transfer instructions
c) branch instructions
d) control transfer & branch instructions

(xxi) The interrupt for which the processor has the highest priority among all the external interrupts is

a) keyboard interrupt
b) TRAP
c) NMI
d) INT

(xxii) The status of the pending interrupts is checked at

a) the end of main program
b) the end of all the interrupts executed
c) the beginning of every interrupt
d) the end of each instruction cycle

(xxiii) The register that may be used as an operand register is

a) Accumulator
b) B register
c) Data register
d) Accumulator and B register

(xxiv) The architecture of 8051 consists of

a) 4 latches
b) 2 timer Registers
c) 4 on-chip I/O ports
d) all of the mentioned

(xxv) The registers that are not accessible by the user are

a) Accumulator and B register
b) IP and IE
c) Instruction registers
d) TMP1 and TMP2

(xxvi) Which of the following is an 8-bit register?

a) PSW(Program Status Word)
b) TCON(Timer Control Register)
c) Accumulator
d) All of the mentioned

(xxvii) What is the clock source for the timers?

a) some external crystal applied to the micro-controller for executing the timer

b) from the crystal applied to the micro-controller

c) through the software

d) through programming

(xxviii) What is the function of the TMOD register?

a) TMOD register is used to set different timer's or counter's to their appropriate modes

b) TMOD register is used to load the count of the timer

c) Is the destination or the final register where the result is obtained after the operation of the timer

d) Is used to interrupt the timer

(xxix) What steps are followed when we need to turn on any timer?

a) load the count, start the timer, keep monitoring it, stop the timer

b) load the TMOD register, load the count, start the timer, keep monitoring it, stop the timer

c) load the TMOD register, start the timer, load the count, keep monitoring it, stop the timer

d) none of the mentioned

(xxx) Which of the following offers external chips for memory and peripheral interface circuits?

a) Microcontroller

b) Microprocessor

c) Peripheral system

d) Embedded system

(xxxi) How is the protection and security for an embedded system made?

a) OTP

b) IPR

c) Memory disk security

d) Security chips

(xxxii) VME bus stands for

a) Versa module Europa bus

b) Versa module embedded bus

c) Vertical module embedded bus
d) Vertical module Europa bus

(xxxiii) Name a volatile memory.

a) RAM
b) EPROM
c) ROM
d) EEPROM

(xxxiv) The initial routine is often referred to as

a) Initial program
b) Bootstrap program
c) Final program
d) Initial embedded program

(xxxv) Which one of the following is UV erasable?

a) Flash memory
b) SRAM
c) EPROM
d) DRAM

(xxxvi) Which type of memory is suitable for low volume production of embedded systems?

a) ROM
b) Volatile
c) Non-volatile
d) RAM

(xxxvii) What type of memory is suitable for high volume production?

a) RAM
b) ROM
c) EPROM
d) EEPROM

(xxxviii) How the input terminals are associated with external environments?

a) Actuators
b) Sensors
c) Inputs
d) Outputs

(xxxix) Which register set of 80286 form the same register set of 8086 processor?

a) AH,AL
b) BX
c) BX,AX
d) EL

(xl) Which are the 4 segmented registers in intel 80286?

a) AX,BX,CX,DX
b) AS,BS,CS,DS
c) SP,DI,SI,BP
d) IP,FL,SI,DI

(xli) What is the size of the address bus in 80286?

a) 20
b) 24
c) 16
d) 32

(xlii) What is 80/20 rule?

a) 80% instruction is generated and 20% instruction is executed
b) 80% instruction is executed and 20% instruction is generated
c) 80%instruction is executed and 20% instruction is not executed
d) 80% instruction is generated and 20% instructions are not generated

(xliii) How is memory accessed in RISC architecture?

a) load and store instruction
b) opcode instruction
c) memory instruction
d) bus instruction

(xliv) Which of the following processors uses Harvard architecture?

a) TEXAS TMS320
b) 80386
c) 80286
d) 8086

(xlv) Princeton architecture is also known as

a) von Neumann architecture
b) Harvard
c) RISC
d) CISC

(xlvi) Which of the following is more quickly accessed?

a) RAM
b) Cache memory
c) DRAM
d) SRAM

(xlvii) Which of the following determines a high hit rate of the cache memory?

a) size of the cache
b) number of caches
c) size of the RAM
d) cache access

(xlviii) Which factor determines the number of cache entries?
a) set commutativity
b) set associativity
c) size of the cache
d) number of caches

(xlix) Which factor determines the cache performance?
a) Software
b) peripheral
c) input
d) output

(l) What does DMA stand for?
a) direct memory access
b) direct main access
c) data main access
d) data memory address

(li) Who has invented flash memory?
a) Dr.Fujio Masuoka
b) John Ellis
c) Josh Fisher
d) John Ruttenberg

(lii) Which is the early form of non-volatile memory?
a) magnetic core memory
b) ferrimagnetic memory
c) anti-magnetic memory
d) anti-ferromagnetic

(liii) In which memory, the signals are multiplexed?
a) DRAM
b) SRAM
c) EPROM
d) EEPROM

(liv) Which of the following has programmable hardware?
a) microcontroller
b) microprocessor
c) coprocessor
d) FPGA

(lv) Which of the following defines the number of samples that are taken in the time period?

a) sample size
b) sample nature
c) sample rate
d) sample frequency

(lvi) Which of the following can determine the maximum frequency that can be converted?

a) sample frequency
b) sample rate
c) sample size
d) sample nature

(lvii) Which of the following introduce a phase error?

a) conversion time
b) sampling rate
c) sample size
d) sample nature

(lviii) Which filter is used for filtering out the high frequency components?

a) bandpass filter
b) band reject filter
c) analogue filter
d) digital filter

(lix) During the execution of instructions, if an instruction is executed, then next instruction is executed only when the data is read by

a) control unit
b) bus interface unit
c) execution unit
d) cpu

(lx) The type of execution which means that the CPU should speculate which of the next instructions can be executed earlier is

a) speculative execution
b) out of turn execution
c) dual independent bus
d) multiple branch prediction

(lxi) A dual independent bus has

a) Enhanced system bandwidth
b) CPU that can access both cache and memory simultaneously

c) High throughput
d) All of the mentioned

(lxii) Which of the following is not an independent engine of Pentium-Pro?

a) fetch-decode unit
b) dispatch-execute unit
c) control-execute unit
d) retire unit

(lxiii) Which processor has the necessity of manual optimization for the generation of assembly language code especially for the embedded systems?

a) RISC
b) CISC
c) Both RISC & CISC
d) none of the mentioned

(lxiv) Which part of the software is transparent to the interrupt mechanism?

a) background
b) foreground
c) both background and foreground
d) lateral ground

(lxv) The time taken to respond to an interrupt is known as

a) interrupt delay
b) interrupt time
c) interrupt latency
d) interrupt function

(lxvi) Data Bus of 8085 ----------

a) 12 bits
b) 10 bits
c) 8 bytes
d) none of above

(lxvii) No of Mode in PPI ic 8255 .....

a) 4
b) 5
c) 7
d) None

(lxviii) No of pin in ic 8255

a) 6
b) 8
c) 4
d) None of Above

(lxix)

Power supply of 8086 ic

a) 100v
b) 60v
c) 1000v
d) None of above

(lxx) Clock in 8085

a) sine
b) Cosine
c) impulse
d) None of Above