BRAINWARE UNIVERSITY
Term End Examination 2020 - 21
Programme – Diploma in Electronics & Communication Engineering
Course Name – Industrial Electronics I
Course Code - DECE504
Semester / Year - Semester V

Time allotted : 85 Minutes   Full Marks : 70

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question)   1 x 70=70

1.   *(Answer any Seventy)*

(i) Which of the following devices does not belong to the transistor family?

a) IGBT   b) MOSFET
c) GTO   d) BJT

(ii) In a power transistor, _____ is the controlled parameter.

a) VCE   b) VBE
c) IB   d) IC

(iii) In a power transistor, _____ is the controlling parameter.

a) VCE   b) VBE
c) IB   d) IC

(iv) For a power transistor, if the base current IB is increased keeping VCE constant, then

a) IC increases   b) IC decreases
c) IC remains constant   d) none of these

(v)

The value of β is given by the expression

a) IC/IB

b) IC/IE

c) IE/IC

d) IE/IB

(vi)

For a power transistor, if the forward current gain $\alpha = 0.97$, then $\beta = ?$

a) 0.03

b) 2.03

c) 49.24

d) 32.33

(vii) For a power transistor, which of the following relations is true?

a) Ie>Ic>Ib

b) Ib>Ic>Ie

c) Ic>Ie>Ib

d) Ie=Ib

(viii) The instantaneous power loss during the delay time of a transistor is given by

a) Ic Vce

b) Ib Vbe

c) Ic Vbe

d) Ib Vce

(ix) A 1mv of i/p gives an output of 1V, the voltage gain as such would be

a) 0.001

b) 0.0001

c) 1000

d) 100

(x) Choose the correct statement

a) A transistor will remain on as long the the base current is applied

b) A transistor remains on after a high to low pulse is applied at the base

c) A transistor will remain on as long the the collector current is applied

d) A transistor remains on after a high to low pulse is applied at the collector

(xi) A thyristor (SCR) is a
    a) P-N-P device   b) N-P-N device
    c) P-N-P-N device   d) P-N device

(xii) Choose the false statement.
    a) SCR is a bidirectional device   b) SCR is a controlled device
    c) In SCR the gate is the controlling terminal   d) SCR are used for high-power applications 1280µs

(xiii) For an SCR in the forward blocking mode (practically)
    a) leakage current does not flow   b) leakage current flows from anode to cathode
    c) leakage current flows from cathode to anode   d) leakage current flows from gate to anode

(xiv) For a forward conducting SCR device, as the forward anode to cathode voltage is increased
    a) the device turns on at higher values of gate current   b) the device turns on at lower values of gate current
    c) the forward impedance of the device goes on increasing   d) the forward impedance of the device goes on decreasing

(xv) Usually the forward voltage triggering method is not used to turn-on the SCR because
    a) it increases losses   b) it causes noise production
    c) it may damage the junction & destroy the device   d) relatively it's an inefficient method

(xvi) The forward break over voltage is maximum when
    a)   b) Gate current $= 0$

Gate current = ∞

c)   d) It is independent of gate current

Gate current = -∞

(xvii) The value of anode current required to maintain the conduction of an SCR even though the gate signal is removed is called as the
    a) holding current   b) latching current
    c) switching current   d) peak anode current

(xviii) _____ are semiconductor thyristor devices which can be turned-on by light of appropriate wavelengths.
    a) LGTOs   b) LASERs
    c) MASERs   d) LASCRs

(xix) For an SCR the total turn-on time consists of i) Delay time ii) Rise time and iii) Spread time During the delay time the
    a) anode current flows only near the gate   b) anode current rises from zero to very high value
    c) losses are maximum   d) anode to cathode voltage is zero

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(xxi) For an SCR the total turn-on time consists of i) Delay time ii) Rise time and the iii) Spread time The spread time interval depends upon
    a) the value of gate current   b) junction temperature

c) area of the cathode   d) area of the anode

(xxii) To avoid commutation failure

  a) circuit turn-off time must be greater than b) circuit turn-off time must be lesser than
the thyristor turn-off time   the thyristor turn-off time

  c) circuit turn-off time must be equal to the d) none of these
thyristor turn-off time

(xxiii) The area under the curve of the gate characteristics of thyristor gives the

  a) total average gate current   b) total average gate voltage

  c) total average gate impedance   d) total average gate power dissipation

(xxiv) Higher the magnitude of the gate pulse

  a) lesser is the time required to inject the b) greater is the time required to inject the
charges   charges

  c) greater is the value of anode current   d) lesser is the value of anode current

(xxv) For an SCR, the gate-cathode characteristic has a slop of 130. The gate
power dissipation is 0.5 watts. Find Ig

  a) 0.62 A   b) 620 mA

  c) 62 mA   d) 6.2 mA

(xxvi) Latching current for an SCR is 100 mA, DC source of 200 V is also
connected from the SCR to the L load. Compute the minimum width of the gate
pulse required to turn on the device. Take $L = 0.2$ H.

  a) 50 micro-sec   b) 100 micro-sec

  c) 150 micro-sec   d) 200 micro-sec

(xxvii) From the two transistor (T1 & T2) analogy of SCR, the total anode
current of SCR is _____ in the equivalent circuit.

  a) the sum of both the base currents   b) the sum of both the collector current

  c) the sum of base current of T1 & collector d) the sum of base current of T2 & collector

current of T2   current of T1

(xxviii)

Latching current for an SCR is 100 mA, a dc source of 200 V is also connected to the SCR which is supplying an R-L load. Compute the minimum width of the gate pulse required to turn on the device. Take L = 0.2 H & R = 20 ohm both in series.

a) 62.7 micro-sec
b) 100.5 micro-sec
c) 56.9 micro-sec
d) 81 micro-sec

(xxix) A fully controlled converter uses

a) diodes only
b) thyristors only
c) both diodes and thyristors
d) none of these

(xxx) A step-down delta-star transformer, with per-phase turns ratio of 5 is fed from a 3-phase 1100 V, 50 Hz source. The secondary of this transformer is connected through a 3-pulse type rectifier, which is feeding feeding an R load. Find the average value of output voltage.

a) 220 V
b) 257 V
c) 650.08 V
d) 206 V

(xxxi) For a 3-phase 6-pulse diode rectifier, has Vml as the maximum line voltage value on R load. The peak current through each diode is

a) Vml/2R
b) 2Vml/R
c) Vml/R
d) Insufficient Data

(xxxii) A 3-phase bridge rectifier charges a 240 V battery. The rectifier is given a 3-phase, 230 V supply. The current limiting resistance in series with the battery is of 8 ohm. Find the average value of battery charging current.

a) 12.56 A
b) 8.82 A
c) 9.69 A
d) 6.54 A

(xxxiii) For a single phase, full bridge, diode rectifier excited from a 230 V, 50 Hz source. With R = 10 ohm & the inductance(L) large enough to maintain continues conduction, the average and rms values of diode currents will be

    a) 7.85 A, 8 A   b) 10.35 A, 7.85 A

    c) 10.35 A, 14.6 A   d) 8 A, 8 A

(xxxiv) The rectification efficiency for B-2 type & M-2 type full wave diode rectifiers are ____ & ____ respectively.

    a)   b)

    $8/\pi$ & $4/\pi$ $4/\pi$ & $8/\pi$

    c)   d)

    $8/\pi$ & $8/\pi$ $4/\pi$ & $4/\pi$

(xxxv) SPMS are based on the _____ principle.

    a) Phase control   b) Integral control

    c) Chopper   d) MOSFET

(xxxvi) _____ is used for critical loads where temporary power failure can cause a great deal of inconvenience.

    a) SMPS   b) UPS

    c) MPS   d) RCCB

(xxxvii) To make a signal diode suitable for high current & high voltage carrying applications with minimum losses, _____

    a) a lightly doped n layer is grown between   b) a heavily doped n layer is grown the two p & n layers   between the two p & n layers

    c) a lightly doped p layer is grown between   d) a heavily doped p layer is grown the two p & n layers   between the two p & n layers

(xxxviii) The V-I Characteristics of the diode lie in the

a) 1st & 2nd quadrant

b) 1st & 3rd quadrant

c) 1st & 4th quadrant

d) Only in the 1st quadrant

(xxxix) A diode is said to be reversed biased when the

a) cathode is positive with respect to the anode

b) anode is positive with respect to the cathode

c) cathode is negative with respect to the anode

d) both cathode and anode are negative

(xl) If V & I are the forward voltage & current respectively, then the power loss across the diode would be

a) V/I

b) V2 I2

c) I2 V

d) VI

(xli) Even after the forward current reduces to zero value, a practical diode continues to conduct in the reverse direction for a while due to the

a) resistance of the diode

b) high junction temperature

c) stored charges in the depletion region

d) none of these

(xlii) In an AC-DC converter, a diode might be used as a

a) voltage source

b) phase angle controller

c) freewheeling Diode

d) filter

(xliii) When the p-n junction diode is reversed biased, the width of the depletion region _____

a) increases

b) decreases

c) remains Constant

d) none of these

(xliv) A triac can be considered as:

a) Two SCRs connected in anti-parallel

b) Two transistors corrected in antiparallel

with a common gate

c) Two SCRs connected in parallel with a common gate

d) Two SCRs connected in parallel with two gates

(xlv) A triac is semiconductor device acting

a) As a diode in the forward direction and SCR in the reverse direction

b) As an SCR in both the directions

c) As diode in both the directions

d) As an SCR in one direction and diode in the other direction

(xlvi) Auxiliary commutation is also known as

a) Class A commutation

b) Class C commutation

c) Class D commutation

d) None of these

(xlvii) In the equilibrium state, the barrier potential across a unbiased silicon diode is _____

a) 0.3 V

b) 0.7 V

c) 1.3 V

d) 0 V

(xlviii) IGBT possess

a) low input impedance

b) high input impedance

c) high on-state resistance

d) second breakdown problems

(xlix) The three terminals of the IGBT are

a) base, emitter & collector

b) gate, source & drain

c) gate, emitter & collector

d) base, source & drain

(l) In IGBT, the p+ layer connected to the collector terminal is called as the

a) drift layer

b) injection layer

c) body layer

d) collector Layer

(li) The controlling parameter in IGBT is the

    a) IG   b) VGE

    c) IC   d) VCE

(lii) The voltage blocking capability of the IGBT is determined by the

    a) injection layer   b) body layer

    c) metal used for the contacts   d) drift layer

(liii) The structure of the IGBT is a

    a) P-N-P structure connected by a MOS gate   b) N-N-P-P structure connected by a MOS gate

    c) P-N-P-N structure connected by a MOS gate   d) N-P-N-P structure connected by a MOS gate

(liv) The static V-I curve of an IGBT is plotted with

    a) Vce as the parameter   b) Ic as the parameter

    c) Vge as the parameter   d) Ig as the parameter

(lv) In an IGBT, during the turn-on time

    a) Vge decreases   b) Ic decreases

    c) Vce decreases   d) None of these

(lvi) The approximate equivalent circuit of an IGBT consists of

    a) a BJT & a MOSFET   b) a MOSFET & a MCT

    c) two BJTs   d) two MOSFETs

(lvii) An IGBT is also know as

    a) MOIGT (Metal oxide insulated gate transistor)   b) COMFET (Conductively modulated FET)

    c) GEMFET (Grain modulated FET)   d) All of these

(lviii) The body of an IGBT consists of a

a) p-layer   b) n-layer

c) p-n layer   d) metal

(lix) At present, the state-of-the-art semiconductor devices are begin manufactured using

a) Semiconducting Diamond   b) Gallium-Arsenide

c) Germanium   d) Silicon-Carbide

(lx) The GTO can be turned off

a) by a positive gate pulse   b) by a negative gate pulse

c) by a negative anode-cathode voltage   d) by removing the gate pulse

(lxi) A GTO can be represented by two transistors T1 & T2. The current gain of both transistors are a1 and a2 respectively. A low value of gate current requires

a) low value of a1 and a2   b) low value of a1 and high value of a2

c) high value of a1 and low value of a2   d) high values of a1 and a2

(lxii) Latching current for the GTOs is _____ as compared to CTs (Conventional thyristors).

a) more   b) less

c) constant   d) cannot be said

(lxiii) In case of the two-transistor model (T1 & T2) of GTO with anode-short, the anode-short is placed between the

a) emitter of T1 & T2   b) emitter of T1 & base of T2

c) emitter of T1 & base of T1   d) emitter of T1 & collector of T2

(lxiv) The Programmable Unijunction Transistor (PUT) turns on & starts conducting when the

a) gate voltage exceeds anode voltage by a   b) anode voltage exceeds gate voltage by a

certain value

c) gate voltage equals the anode voltage

certain value

d) gate is given negative pulse w.r.t to cathode

(lxv) From the following list of devices, choose the device that only turns-on for a fixed-value of anode-cathode voltage

a) PUT

b) SCR

c) SUS

d) BJT

(lxvi) The SCS (Silicon Controlled Switch) is a

a) two terminal device

b) three terminal device

c) four terminal device

d) five terminal device

(lxvii) The SCS is a four layer, four terminal thyristor. Can be turned on by

a) the anode gate

b) the cathode gate

c) either of the gates

d) gating both the gates together

(lxviii) Which of the following devices provide complete isolation between triggering circuit and power circuit?

a) PUT

b) LASCR

c) SUS

d) DIAC

(lxix) The TRIAC can be represented by

a) two SCRs in anti-parallel

b) two SCRs in parallel

c) two diodes in anti-parallel

d) two diodes in parallel

(lxx) The TRIAC's terminals are

a) gate, anode, cathode

b) MT1, MT2, gate

c) gate1, gate2, anode, cathode

d) MT1, MT2, gate1, gate2