18342

BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – M.Tech.(CSE)-AIML-2025
Course Name – Computer Architecture for AI
Course Code - MTA10404
(Semester I)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify the component that distinguishes a microcontroller from a microprocessor.

a) Built-in I/O and memory b) Clock speed
c) Floating-point unit d) GPU interface

(ii) Recognize the main feature of RISC architecture.

a) Complex instructions b) Large instruction set
c) Single-cycle execution d) Multi-cycle decoding

(iii) Describe the behavior of instruction pipelining.

a) Executes one instruction at a time b) Splits instruction execution into stages
c) Uses cache exclusively d) Avoids branch prediction

(iv) Compare ARM and SPARC based on power and architecture.

a) ARM uses CISC while SPARC is RISC b) ARM is low-power and efficient, SPARC is scalable and high-performance
c) SPARC is embedded-friendly d) Both use x86 ISA

(v) Use pipeline depth to compute speedup.

a) Multiply depth by CPI b) Divide depth by stall rate
c) Use ideal speedup = number of stages d) Use loop unrolling factor

(vi) Apply instruction reordering to eliminate pipeline stalls.

a) Swap independent instructions b) Add NOPs before execution
c) Use fixed register names d) Reduce branch frequency

(vii) Utilize Tomasulo's algorithm for hazard resolution.

a) Rename registers statically b) Delay all dependent instructions
c) Use reservation stations with dynamic scheduling d) Execute instructions serially

(viii) Compare pipeline execution before and after loop unrolling.

a) Same number of instructions b) More pipeline bubbles after unrolling

c) Reduced overhead due to fewer branch instructions
d) Increase in cache size

(ix) Compare unified vs split caches for instruction and data.

a) Unified reduces complexity but increases conflicts
b) Split reduces performance
c) Unified avoids cache coherence
d) Split slows both accesses

(x) Implement open-row policy to reduce DRAM latency.

a) Close row after each access
b) Keep row active for multiple accesses
c) Ignore row reuse
d) Refresh entire memory

(xi) Use bank interleaving in memory access.

a) Access same bank repeatedly
b) Access alternating rows
c) Access multiple banks simultaneously
d) Use only L1 cache

(xii) Analyze DRAM controller's role in memory scheduling.

a) Issue requests in fixed order
b) Reorder requests to maximize row hits and minimize conflicts
c) Delay all reads
d) Block writes entirely

(xiii) Identify the core structure of a Tiled Chip Multi-core Processor.

a) Star layout
b) Grid of identical tiles
c) Ring of clusters
d) Randomized node mesh

(xiv) Recognize the component that enables on-chip communication in TCMP.

a) Northbridge controller
b) Global bus
c) Network-on-Chip
d) Shared DMA

(xv) Develop a congestion prediction model for NoC routing.

a) Count failed packets
b) Track recent buffer usage patterns and adjust paths accordingly
c) Delay packets at source
d) Broadcast control signals

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Apply interleaving techniques to secondary storage access. (3)
3. Explain the architecture of a Tiled Chip Multi-core Processor (TCMP). (3)
4. Describe the structure of Superscalar architecture. (3)
5. Analyze the effects of multi-cycle instructions on MIPS pipeline. (3)
6. Evaluate the role of DRAM controllers in reducing memory access delays. (3)

OR

Assess the reliability of magnetic hard disks vs solid-state drives. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain the design principles and advantages of TCMP. (5)
8. Propose a power-efficient router design for energy-aware NoC architecture. (5)
9. Apply instruction scheduling techniques to eliminate pipeline stalls. (5)
10. Analyze Tomasulo's algorithm components and its role in ILP. (5)
11. Analyze the performance difference between direct-mapped and fully associative cache. (5)
12. Analyze DRAM controller architecture and scheduling mechanisms. (5)

OR

Compare multiple DRAM address mapping techniques. (5)

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