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BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – B.Tech.(CSE)-2024/B.Tech.(CSE)-AIML-2024/B.Tech.(CSE)-DS-2024/B.Tech.(CSE)-AIR-2024/B.Tech.(CSE)-CYS-2024
Course Name – Computer Organization and Architecture
Course Code - BTS30101/BTA30101/BTD30101/BTR30101/BTY30101
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) The mantissa of the fraction in IEEE 32-bit representations of memories is said to occupy _______ bits.

a) 24 b) 23
c) 18 d) 32

(ii) Convert the binary number (1111000011110000) to hexadecimal number

a) 1010 b) F0F0
c) 7070 d) 5050

(iii) Apply signed-magnitude binary division and find the result if the dividend is (11100)2 and divisor is (10011)2

a) 10100 b) 100
c) 11001 d) 1100

(iv) Identify the formula for the Hit Ratio

a) Hit/(Hit + Miss) b) Miss/(Hit + Miss)
c) (Hit + Miss)/Miss d) (Hit + Miss)/Hit

(v) Explain the arithmetic left shift operation as

a) Produces the same result as obtained with logical shift left operation
b) Causes the sign bit to remain always unchanged
c) Needs additional hardware to preserve the sign bit
d) Needs additional hardware to preserve the sign bit

(vi) Select the true statement about the composite unit of the Adder-subtractor

a) It can add as well as subtract two numbers
b) At a time, it either adds or subtracts
c) It mainly operates with parallel adder
d) All of these

(vii) Choose the next level of memory hierarchy after the L2 cache is _______

a) Secondary storage
b) Main memory
c) Register
d) TLB

(viii) Select the memory that is independent of the address bus

a) Secondary memory
b) Main memory
c) Onboard memory
d) Cache memory

(ix) Comparing the time T_1 taken to execute a single instruction on a pipelined CPU with the time T_2 taken on a non-pipelined but otherwise identical CPU, state the correct option

a) T1>T2
b) T1 = T2
c) T1 < T2
d) $T_1 = T_2$ only if the pipeline has no stalls

(x) Identify the functional block that stores data temporarily for execution.

a) CPU
b) Registers
c) ALU
d) BIOS

(xi) Identify the type of CPU register that holds the address of the next instruction.

a) Program Counter
b) Accumulator
c) IR
d) Status Register

(xii) Identify the term that describes the combination of control signals and register operations.

a) Instruction Cycle
b) RTL
c) ALU Operation
d) Instruction Format

(xiii) Identify the multiplication algorithm suitable for signed binary numbers.

a) Decimal Multiplier
b) Booth Algorithm
c) Carry-Save Adder
d) Shift-Add

(xiv) Illustrate the Memory management technique where allocated size is fixed -

a) paging
b) segmentation
c) fragmentation
d) indexing

(xv) Interpret the type of memory that is/are the type of multi-processor based on memory

a) Shared memory
b) Distributed memory
c) Both of these
d) None of these

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Assuming the registers are zero initially. Identify the the content of R1 after the following instructions sequence is executed. MOV R1,#6 MOV R2,#5 ADD R3,R1,R1 SUB R1,R3,R2 MULT R3,R1,R1 (3)
3. A hierarchical cache-main memory subsystem has the following specifications: i. Cache access time of 160 ns ii) main memory access time of 960 ns iii) hit ratio of cache memory is 0.9. Calculate the average access time of the memory system. (3)
4. State any one methods of binary division with an example. (3)
5. Define DMA. (3)
6. Illustrate the difference between interrupt service routine and subroutines (3)

OR

Estimate the steps involved in an instruction cycle. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Compare the characteristics of SRAM(Static RAM) and DRAM(Dynamic RAM). Evaluate the choice between SRAM and DRAM impact on memory system design. (5)
8. Explain the overflow and underflow problems in floating-point representation. (5)
9. State Von Neumann architecture with block diagram. (5)

10. Illustrate why CLA is called fast parallel adder. (5)
11. Illustrate the importance of I/O buffering in computer systems. (5)
12. "Consider the page reference string as 3, 1, 2, 1, 6, 5, 1, 3 with 3-page frames. Evaluate the number of page faults using FIFO, LRU" (5)

OR

Judge the significance of Page Replacement Algorithms? (5)

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